

# Iris HSW/BDW Schematics

## Broadwell-ULT

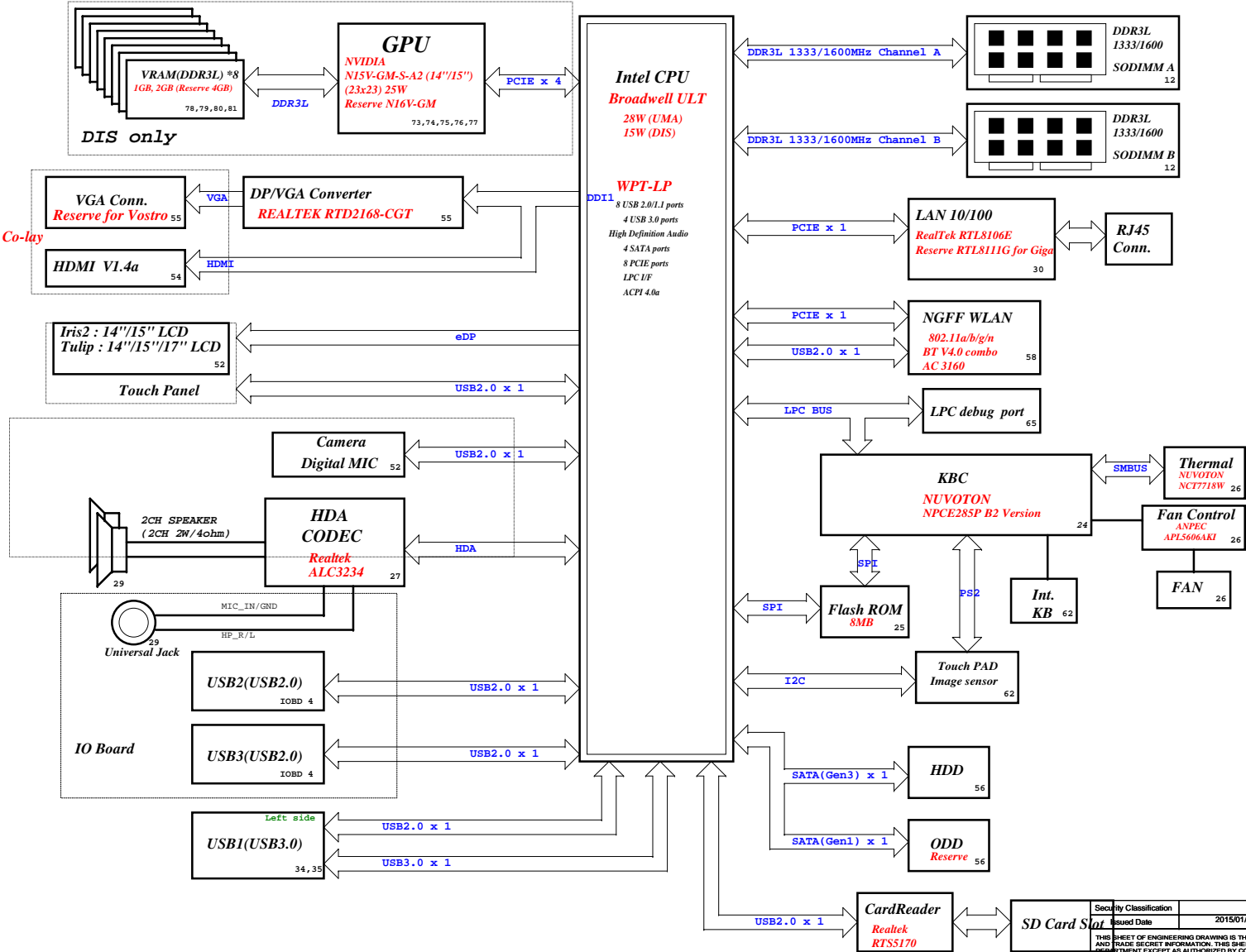
2015-01-20  
REV : A00

DY : None Installed  
UMA: UMA only installed  
OPS: DISCRTE OPTIMUS installed

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Date: Wednesday, January 21, 2015		Sheet 1 of 102			

Project code:  
Iris-2 14 --> 4PD031010001  
Iris-2 15 --> 4PD032010001  
PCB P/N: 14216  
Revision: X01

Iris2/Tulip/VanGogh Block Diagram



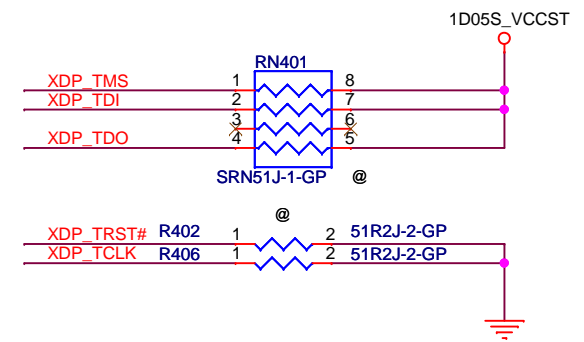
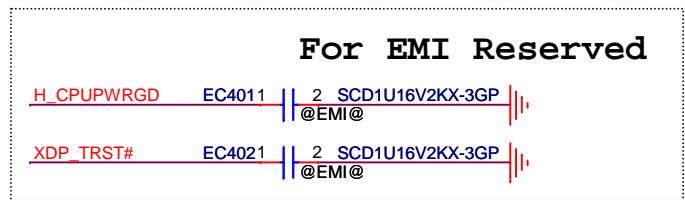
CHARGER	
HFA0224RGRR-1-GP	44
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT
SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	3D3V AUX_S5 5V AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95813HRZ-GP	46,47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR3L SUS	
TPS51716RUKR-GP	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0
CPU 1.05V	
RT8237CZQW-2-GP	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
CPU 1D5V_S0	
TLV70215DBVR-GP	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
Switches	
INPUTS	OUTPUTS
1D35V_S3 5V_S5 3D3V_S5 1D05V_S0 3D3V_S0 1D35V_S3	1D35V_S0 5V_S0 3D3V_S0 1D05V_VGA_S0 3D3V_VGA_S0 1D35V_VGA_S0
PCB LAYER	
L1:Top L2:VCC L3:Signal L4:Signal L5:GND L6:Signal	

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( Blanking )

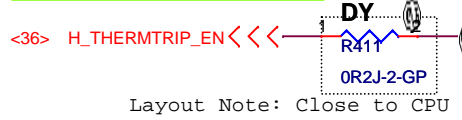
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						Size		Document Number		Rev	
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Main Func = CPU

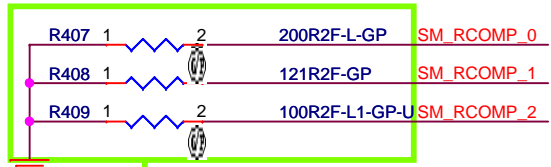
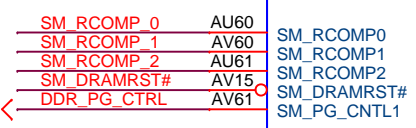


Layout Note:

Impedance control:50 ohm

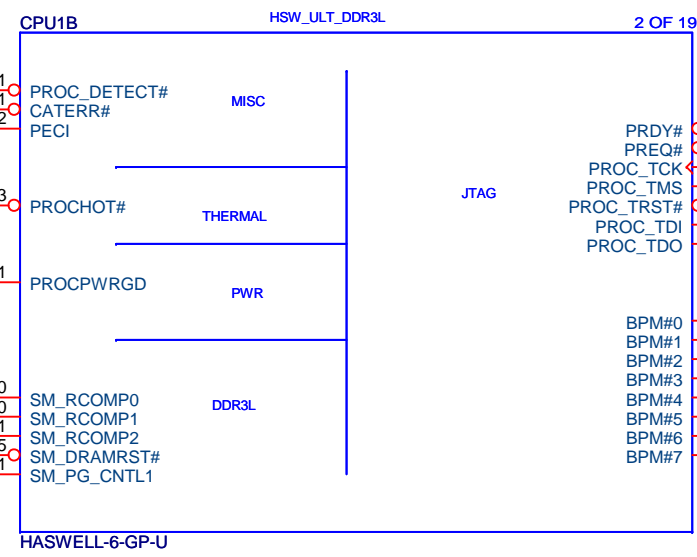


Layout Note: Close to CPU



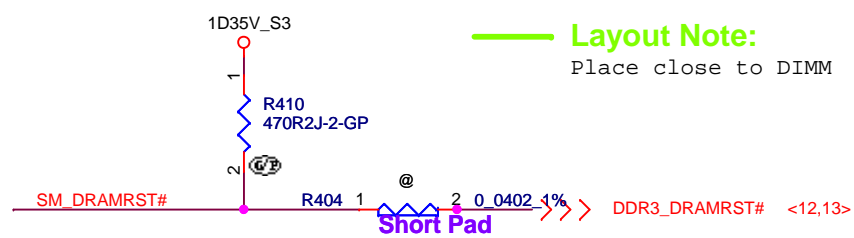
Layout Note:

Design Guideline:  
SM\_RCOMP keep routing length less than 500 mils.

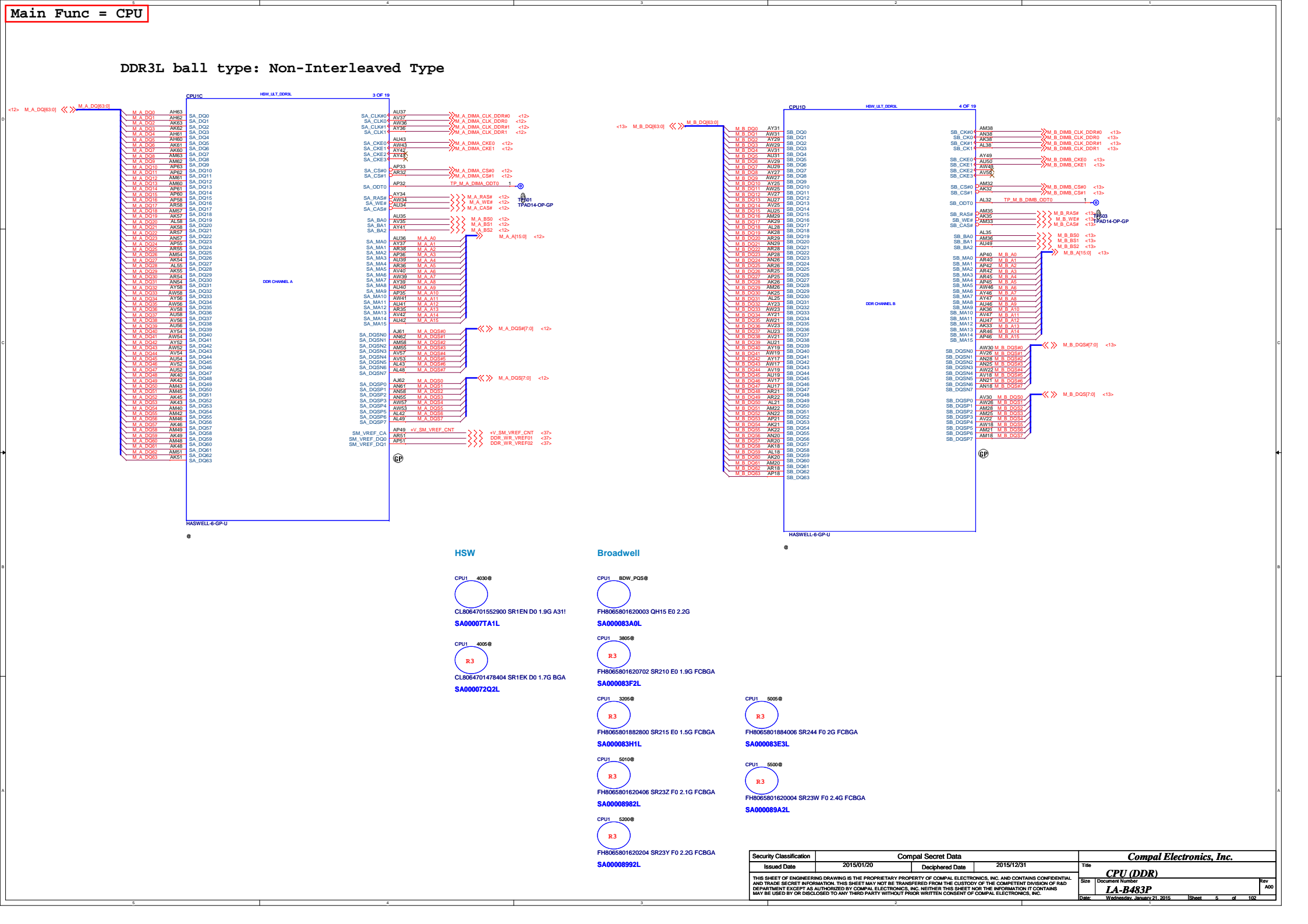


Layout Note:

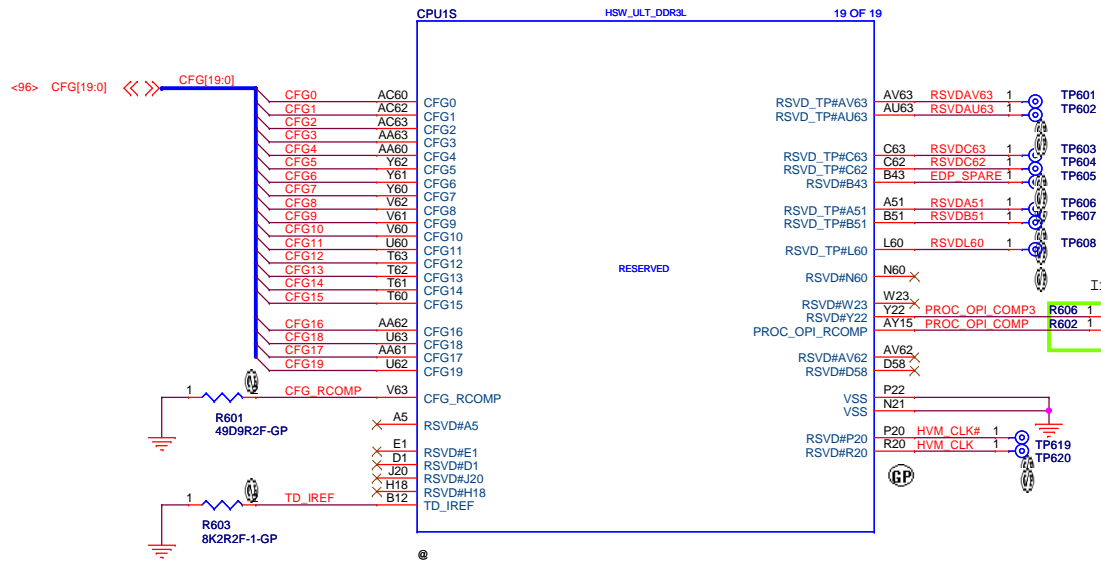
Place close to DIMM



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102					



Main Func = CPU



7.4 Reserved or Unused Signals

- The following are the general types of reserved (RSVD) signals and connection guidelines:
- RSVD – these signals should not be connected
  - RSVD\_TP – these signals should be routed to a test point
  - RSVD\_NCTF – these signals are non-critical to function and may be left unconnected

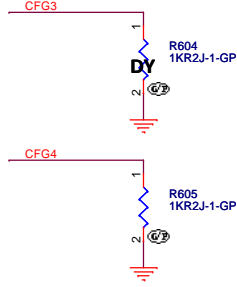
Intel Recommend

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

#514405 PCH strap pin:

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	<p><b>Configuration Signals:</b> The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none"><li>• <b>CFG[2:0]:</b> Reserved configuration lane. A test point may be placed on the board for these lanes.</li><li>• <b>CFG[3]: MSR Privacy Bit Feature</b><ul style="list-style-type: none"><li>– 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting</li><li>– 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden</li></ul></li><li>• <b>CFG[4]: eDP enable</b><ul style="list-style-type: none"><li>– 1 = Disabled</li><li>– 0 = Enabled</li></ul></li><li>• <b>CFG[19:5]:</b> Reserved configuration lanes. A test point may be placed on the board for these lanes.</li></ul>	I/O GTU



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT



D

C

B

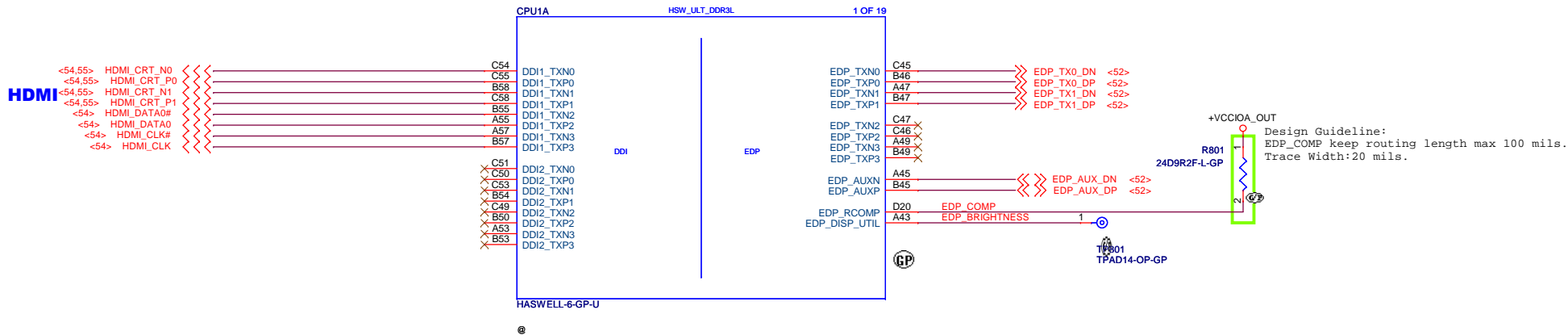
A

D

C

B

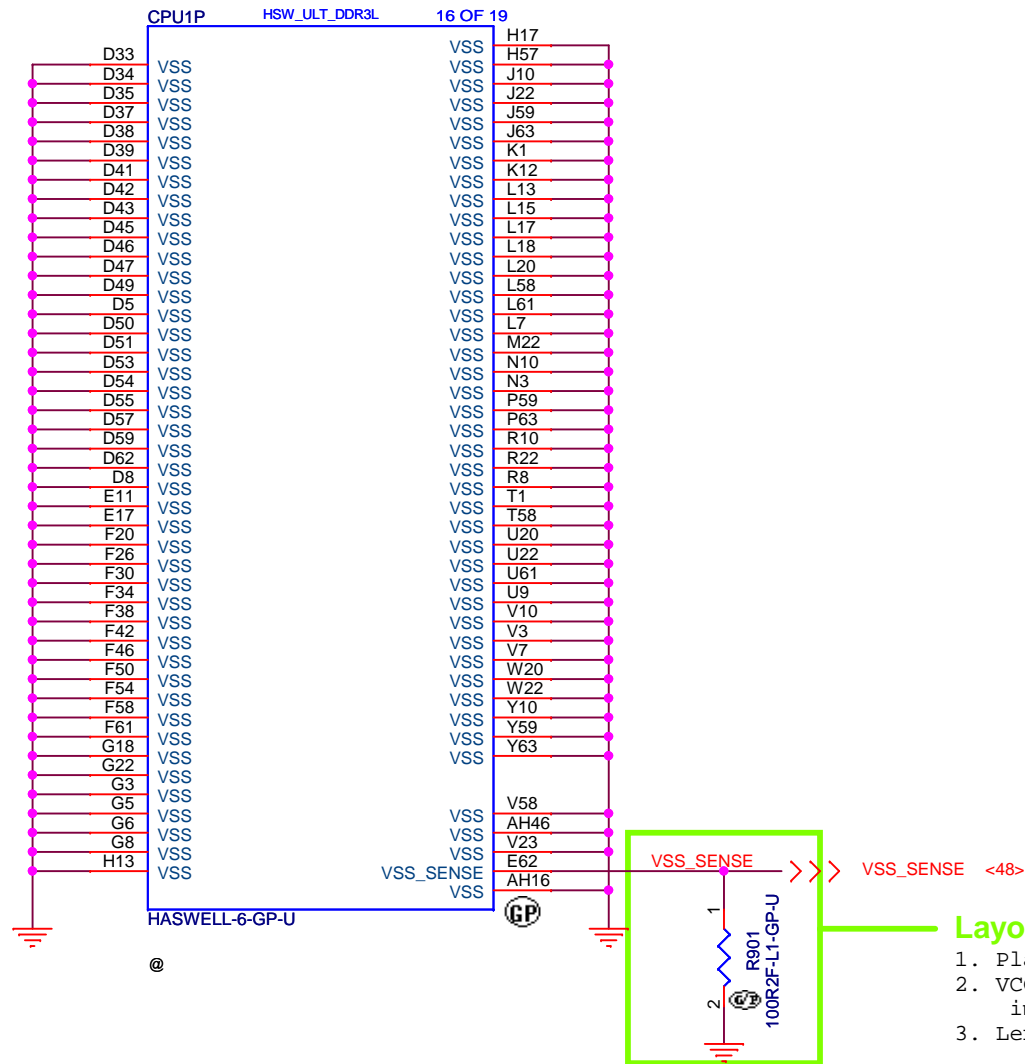
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Main Func = CPU

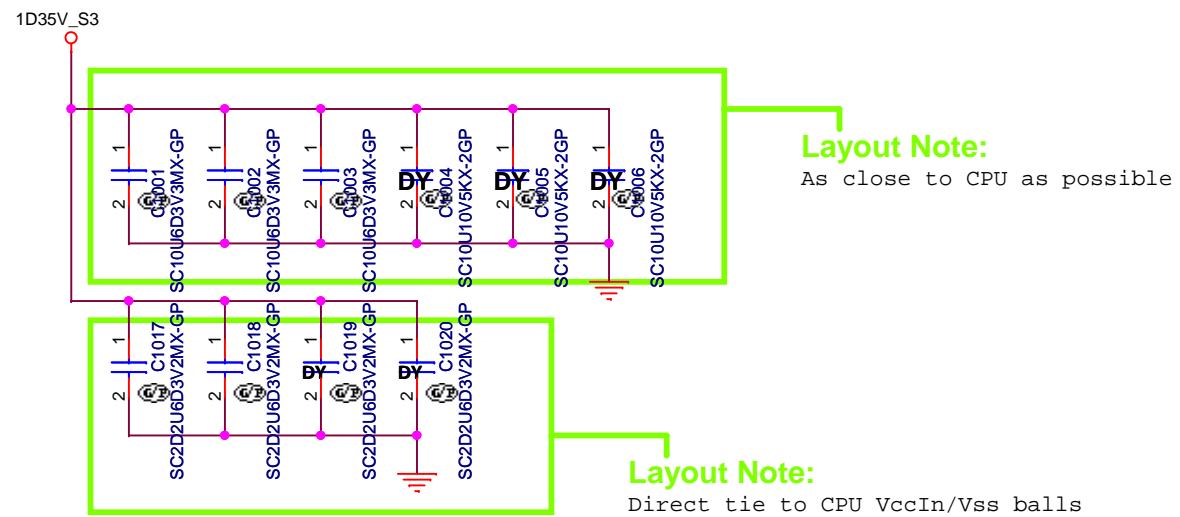


Layout Note:

- 1. Place close to CPU
- 2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
- 3. Length match<25mil

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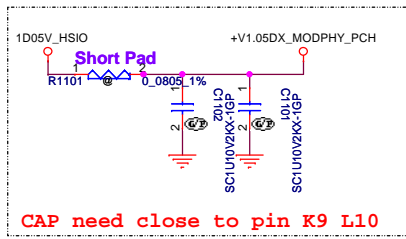
Main Func = CPU



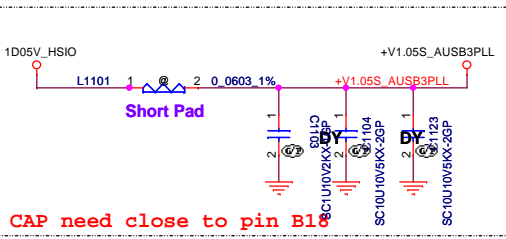
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MAX: 1.92A

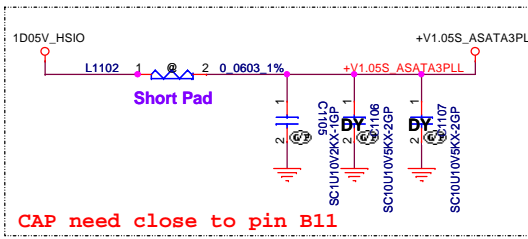
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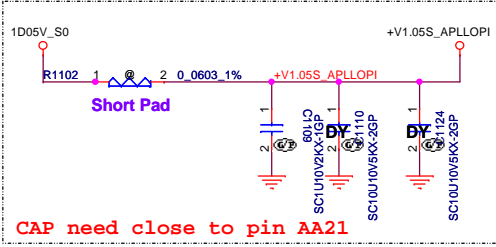
41mA



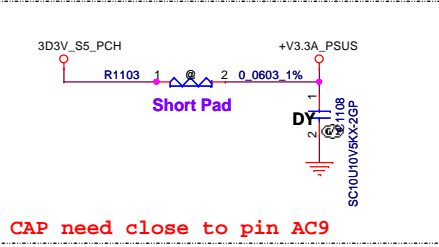
42mA



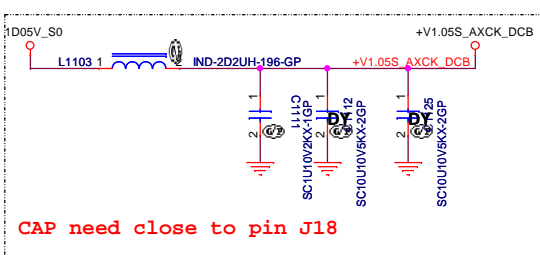
57mA



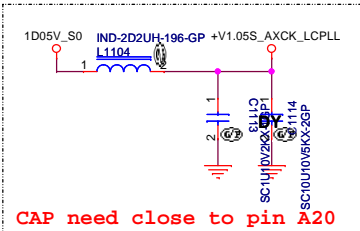
62mA



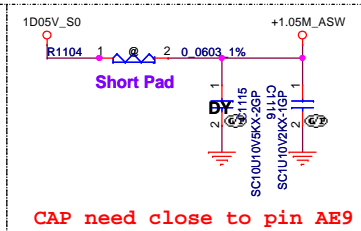
185mA



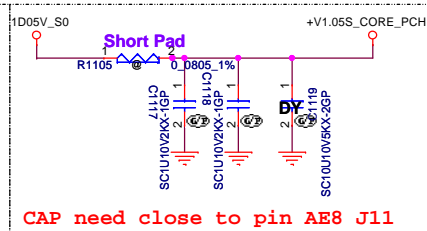
31mA



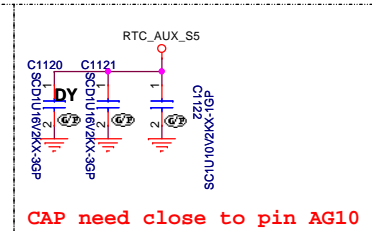
658mA

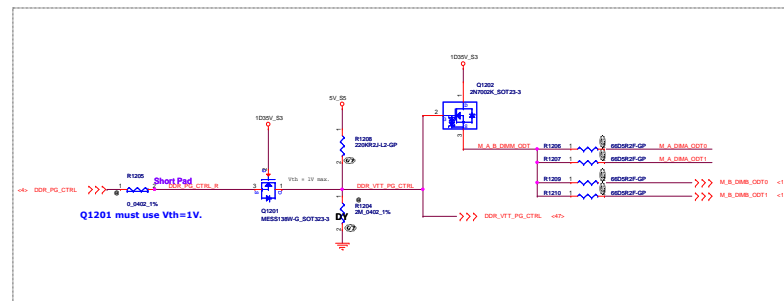
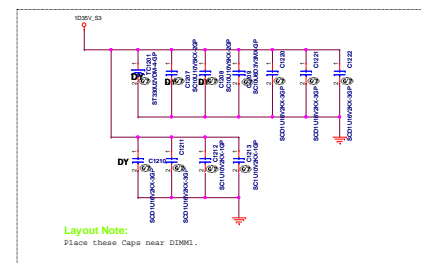
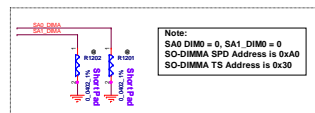
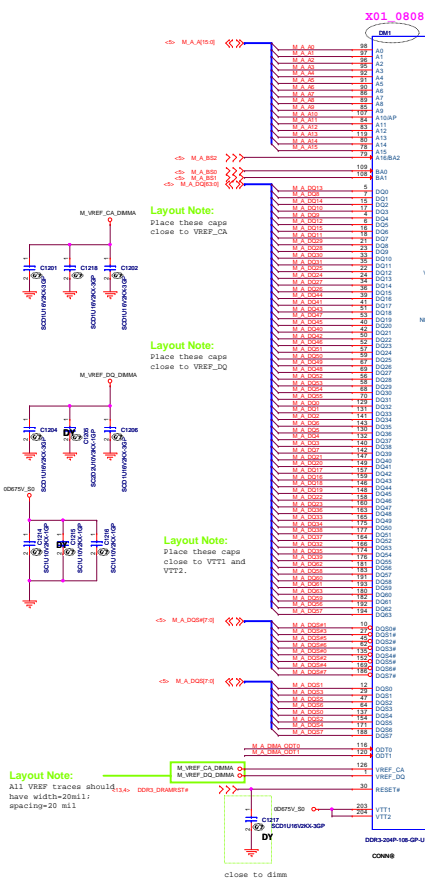


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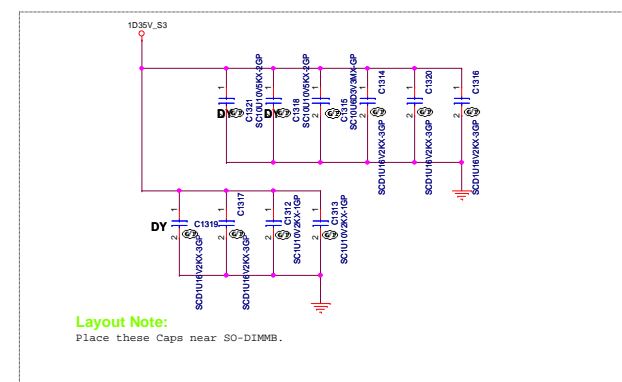
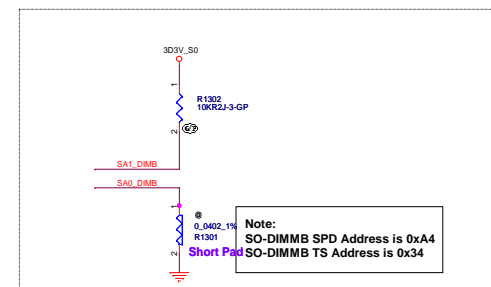
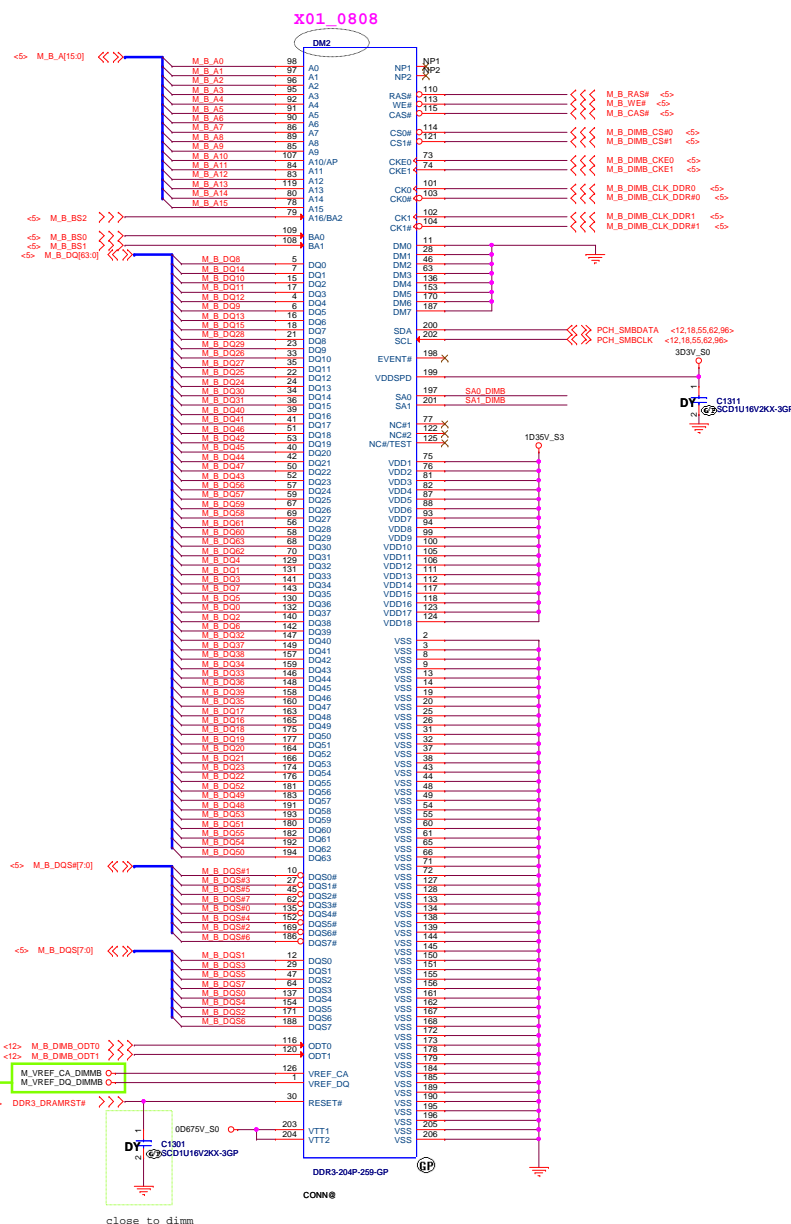
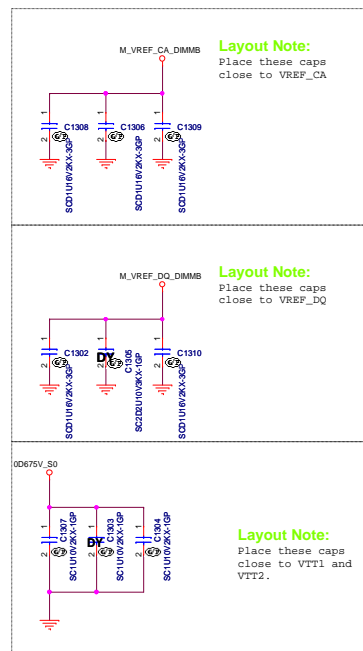


1mA





5  
Main Func = DIMM2

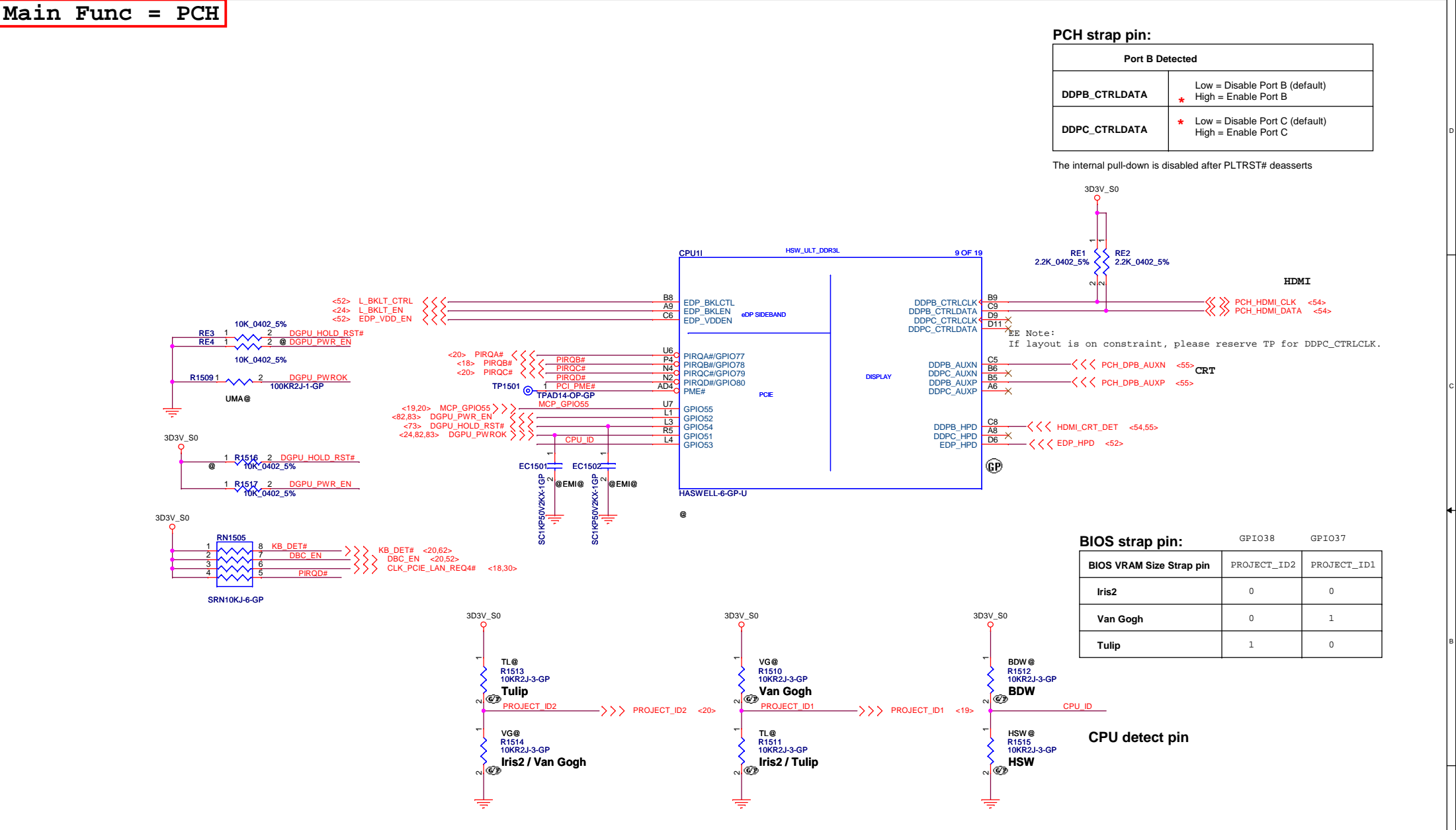


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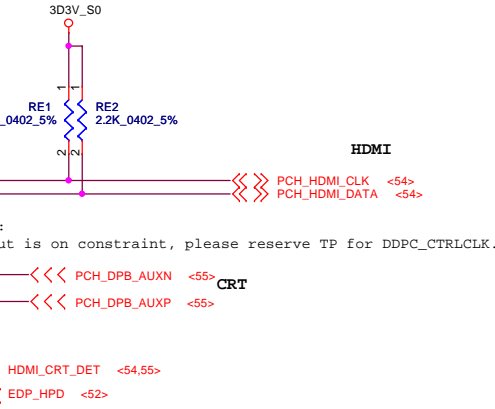
Main Func = PCH



PCH strap pin:

Port B Detected	
DDPB_CTRLDATA	Low = Disable Port B (default) ★ High = Enable Port B
DDPC_CTRLDATA	★ Low = Disable Port C (default) High = Enable Port C

The internal pull-down is disabled after PLTRST# deasserts

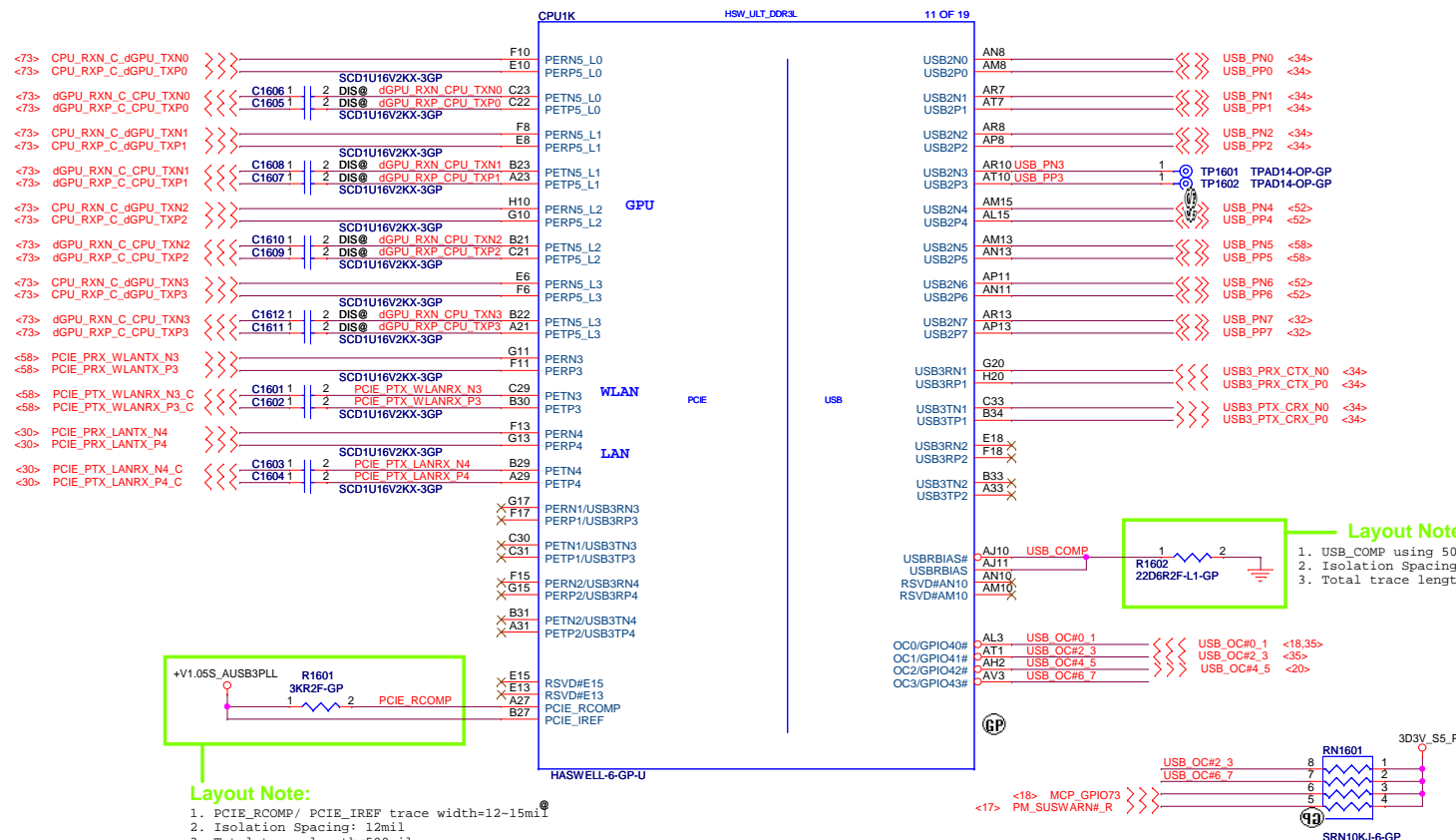


BIOS strap pin:

BIOS VRAM Size Strap pin	PROJECT_ID2	PROJECT_ID1
Iris2	0	0
Van Gogh	0	1
Tulip	1	0

CPU detect pin

Main Func = PCH



USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB2.0 Port2 (Debug Port/IOBD)
2	USB2.0 Port3 (IOBD)
3	X
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5(L0~L3)	GPU	
6(L3)	HDD	SATA0
6(L2)	ODD	SATA1
6(L0~L1)	N/A	

#515621

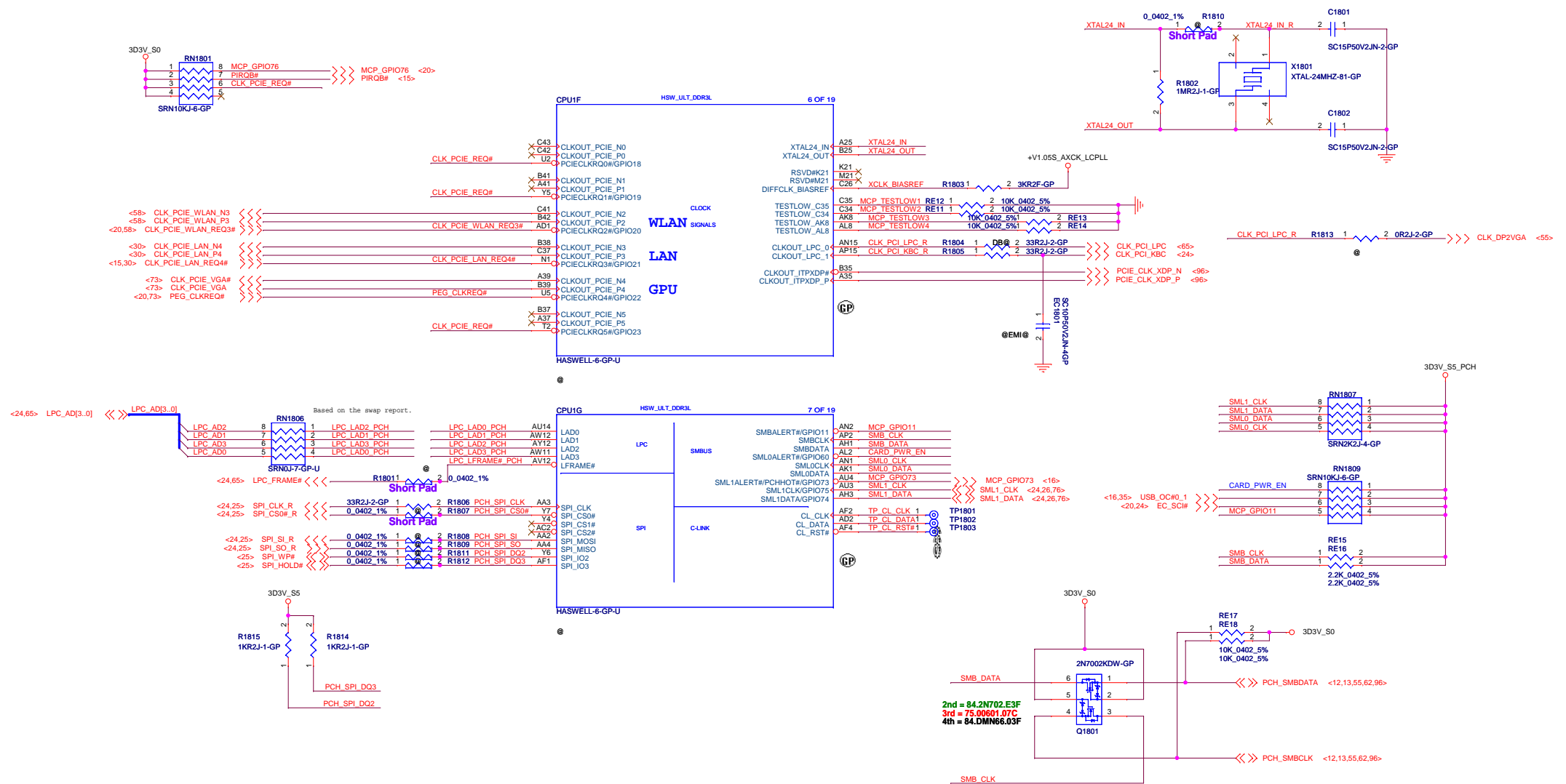
Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU				





## Main Func = PCH

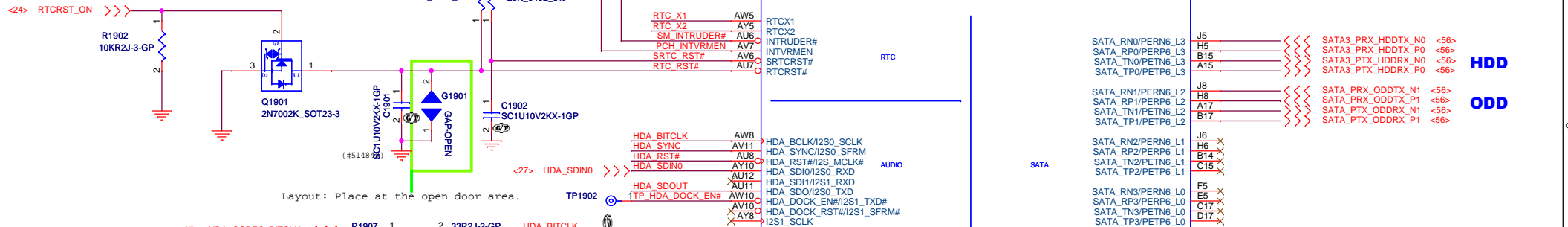
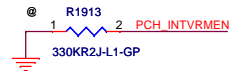


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## Main Func = PCH

**PCH strap pin:**

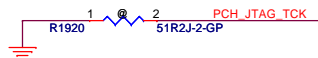
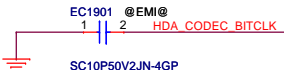
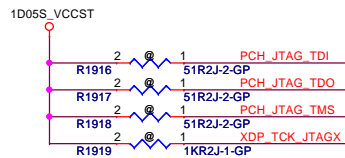
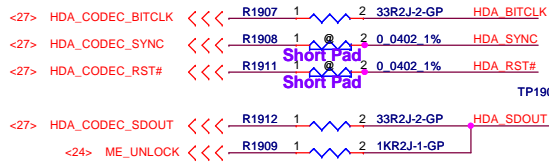
<b>Integrated SUS 1V VRM Enable</b>	
<b>INTVRMEN</b>	Low = External VRs High = Internal VRs*



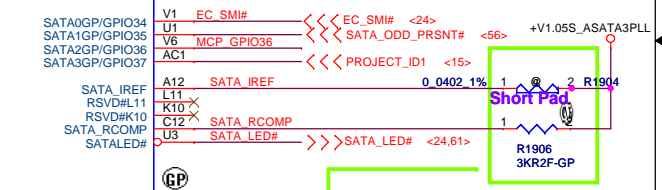
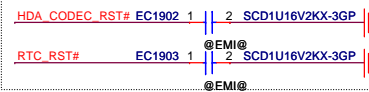
**PCH strap pin:**

<b>Flash Descriptor Security Override/ Intel ME Debug Mode</b>	
<b>HDA_SDOUT</b>	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

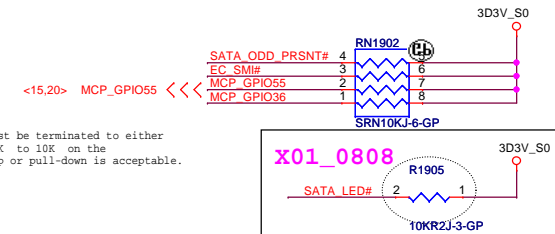


For EMI Reserved



**Layout Note:**

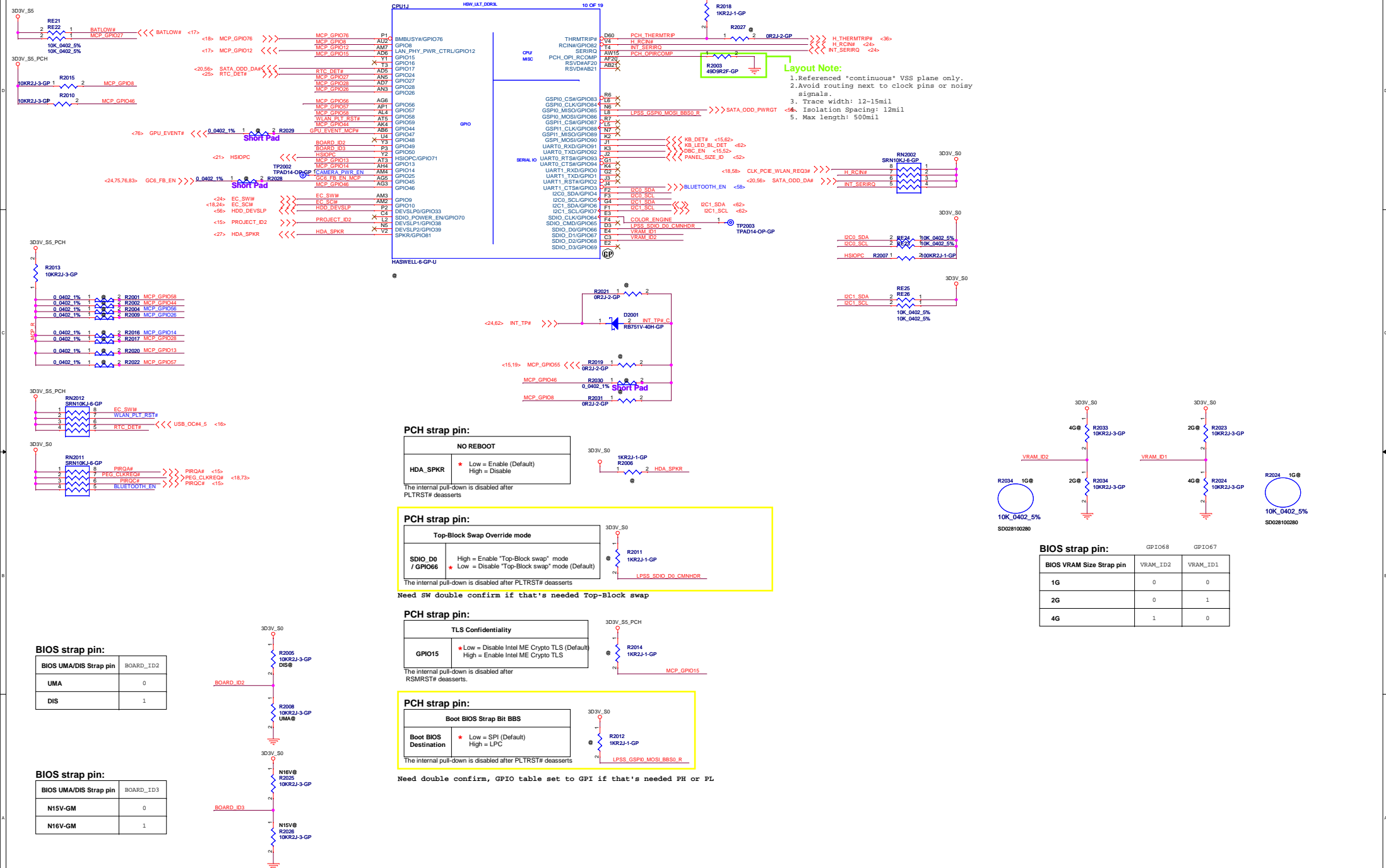
4mil trace at break-out and 3  
12-15mil trace with  $<0.2$  ohms  
and length total  $\leq 500$  mils.



Unused SATA[3:0]GP pins must be terminated to either 3.3V rail or GND using 8.2K to 10K on the motherboard. Either pull-up or pull-down is acceptable.

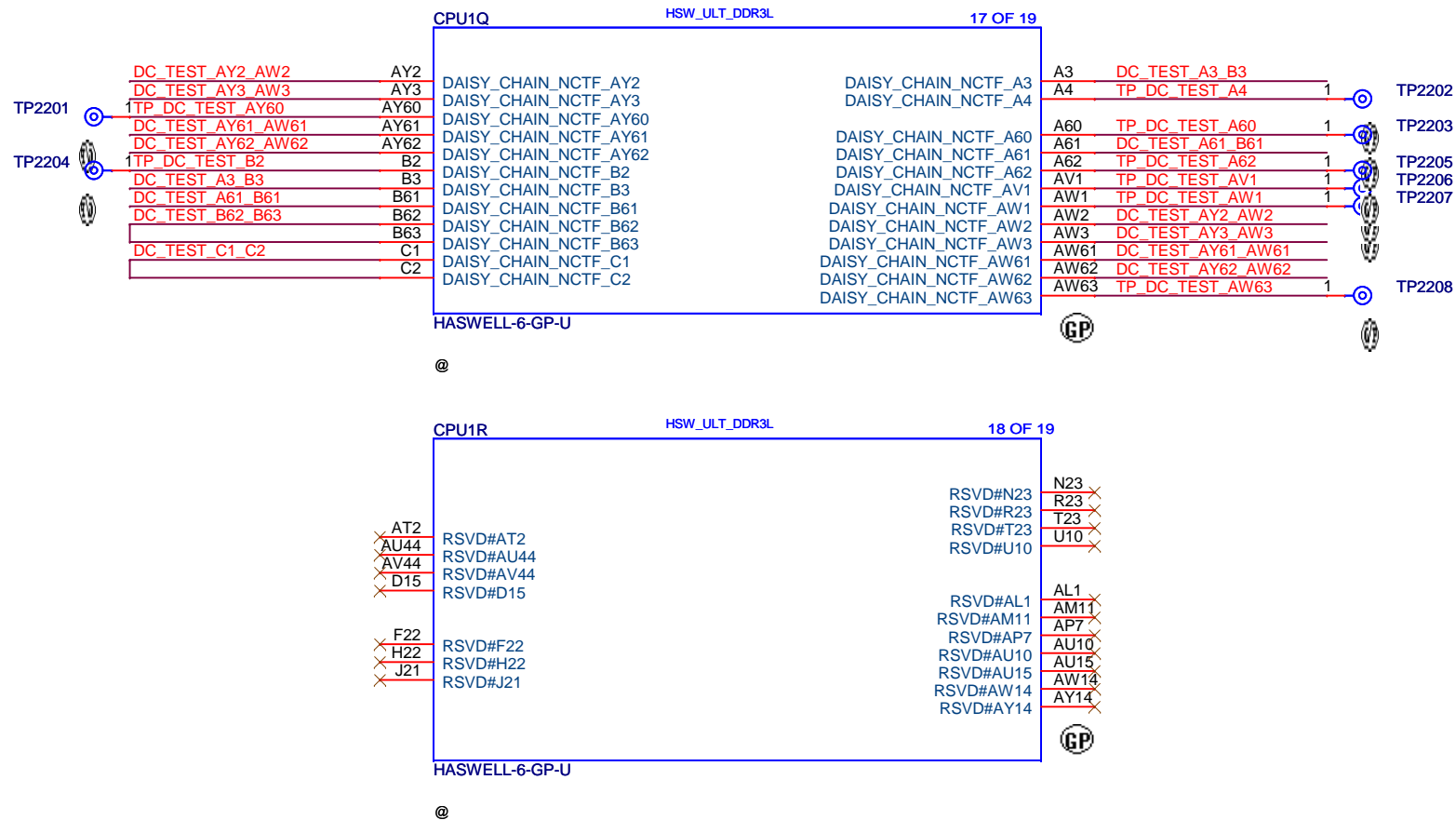
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>CPU (RTC/SATA/IHDA/JTAG)</b>		
Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title		
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					<b>LA-B483P</b>	A00
				Date:	Wednesday, January 21, 2015	Sheet 19 of 102

# Main Func = PCH



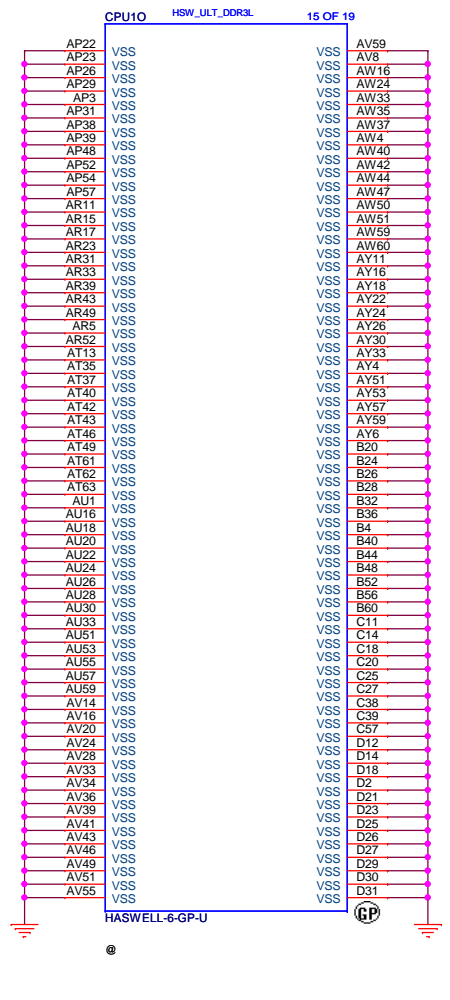
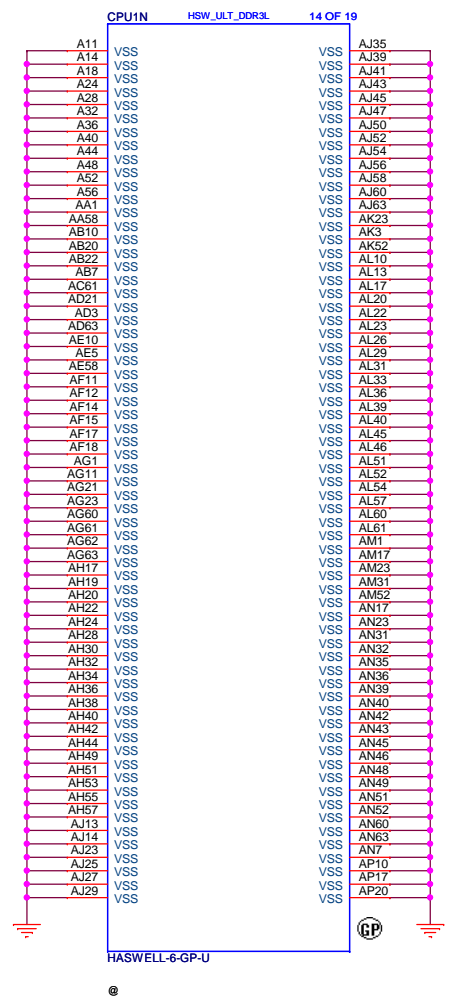


Main Func = PCH

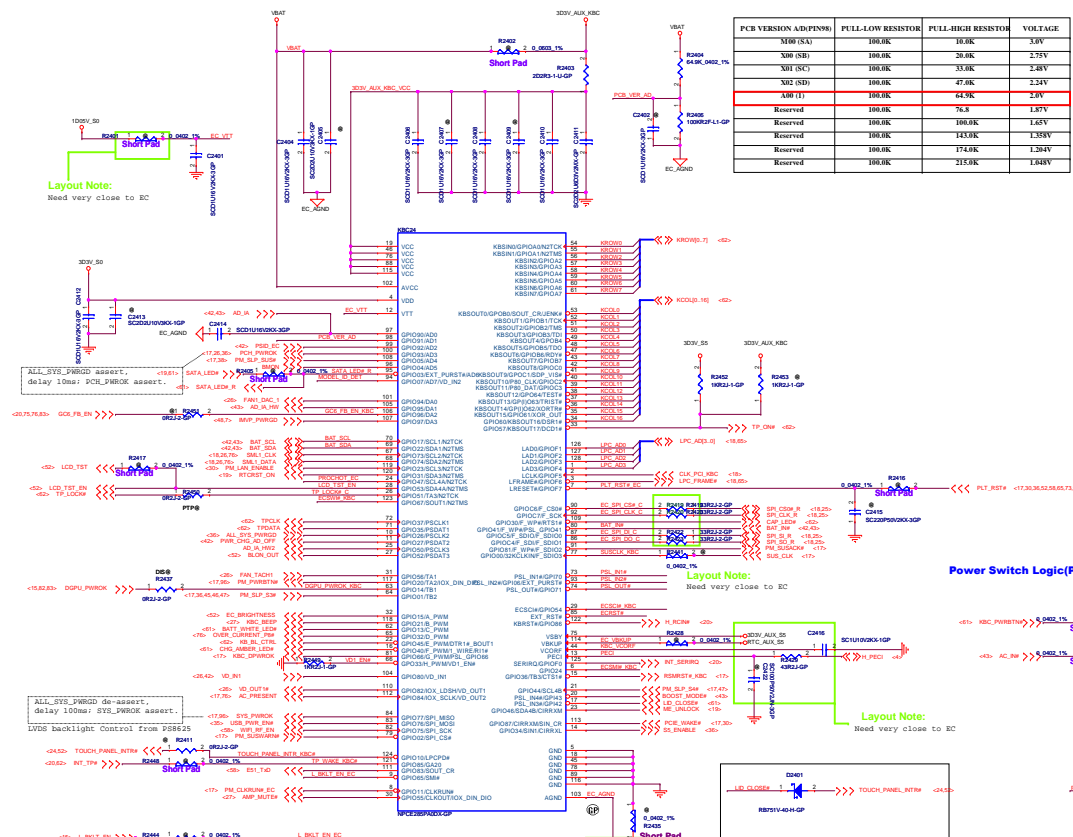


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								Document Number		Rev	
								LA-B483P		A00	
								Date: Wednesday, January 21, 2015		Sheet 22 of 102	

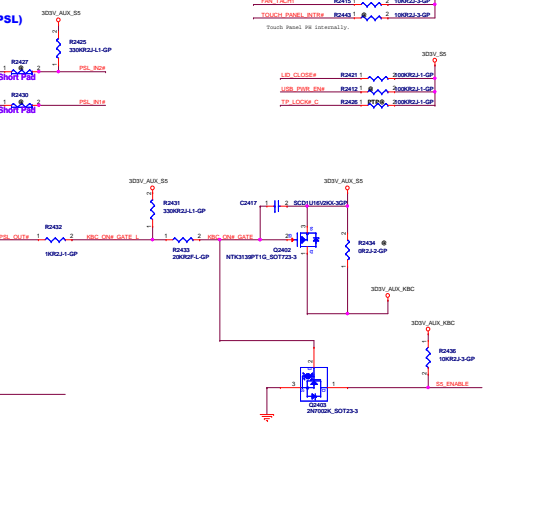
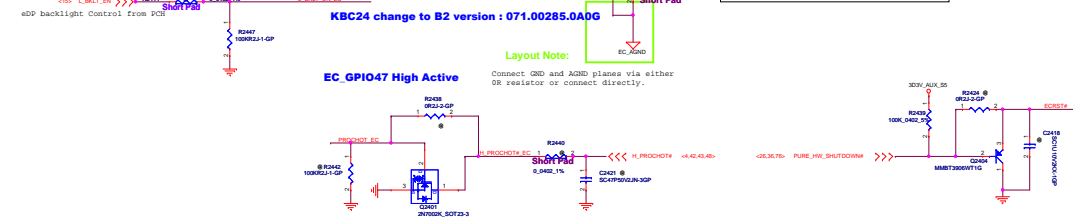
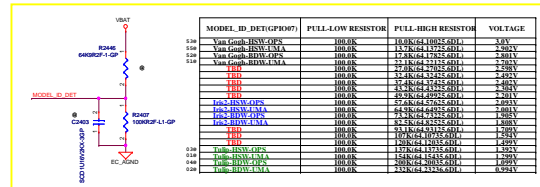
Main Func = PCH



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						Size	Document Number			Rev		
						LA-B483P					A00	
						Date: Wednesday, January 21, 2015					Sheet	23 of 102



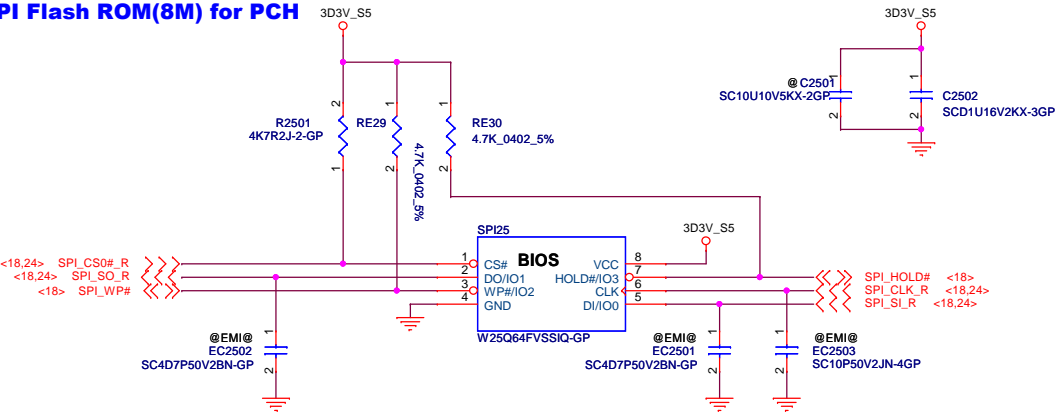
PCB VERSION A(DP)P06	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
M06 (SA)	100.0k	10.0k	3.0V
X00 (SB)	100.0k	20.0k	2.75V
X01 (SC)	100.0k	33.0k	2.48V
X02 (SD)	100.0k	47.0k	2.24V
A00 (1)	100.0k	64.9k	2.0V
Reserved	100.0k	76.8	1.87V
Reserved	100.0k	100.0k	1.65V
Reserved	100.0k	143.0k	1.358V
Reserved	100.0k	174.0k	1.204V
Reserved	100.0k	215.0k	1.048V





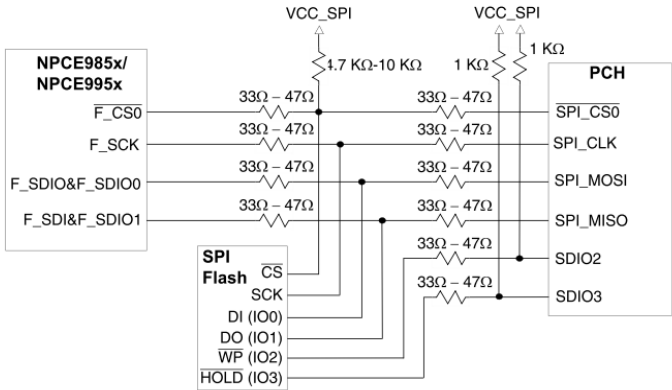
Main Func = SPI Flash

SPI Flash ROM(8M) for PCH



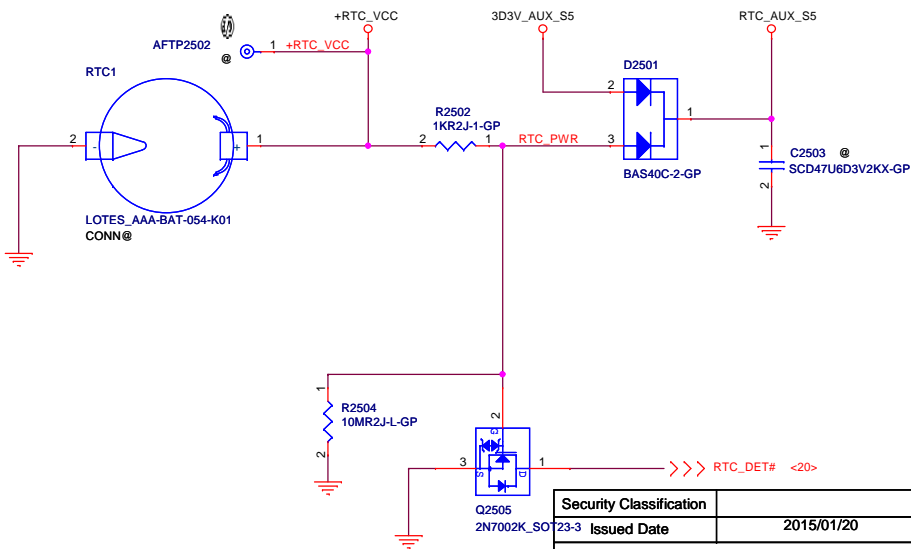
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o
072.25B64.0001	o	o

Single SPI shared flash connection (SPI Quad I/O mode)



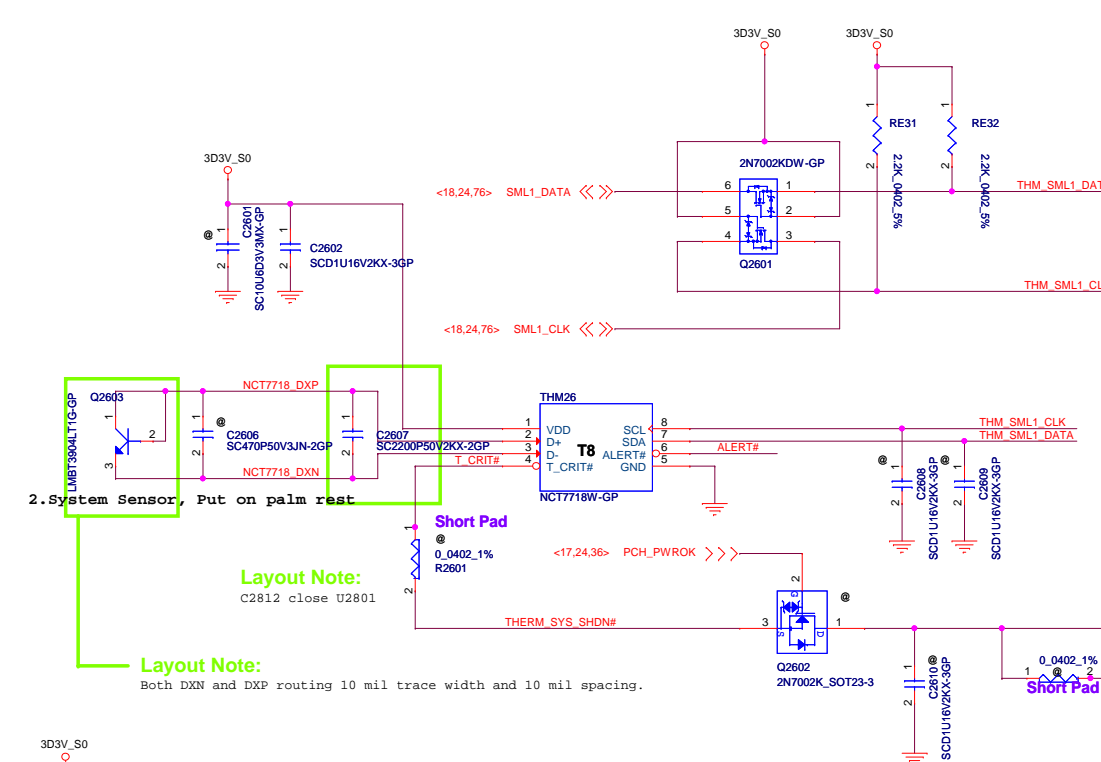
Refer to "NCPE985x/ NPCE995x board design reference guide"

Main Func = RTC

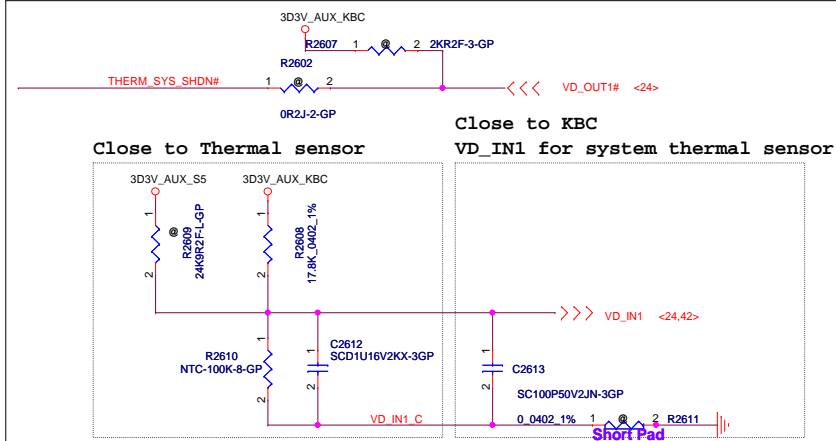


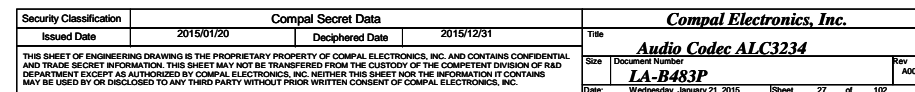
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Issued Date				2015/01/20		Deciphered Date		2015/12/31		Title	
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								LA-B483P		Document Number	
								Wednesday, January 21, 2015		Rev	
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								25		of	
								102			

Main Func = Thermal Sensor



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125





( Blanking )

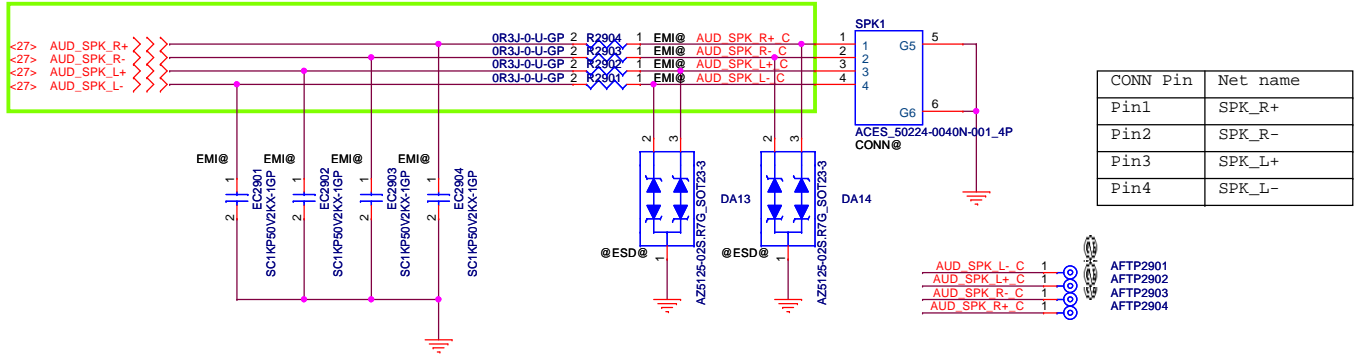
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Reserved		
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				LA-B483P		A00
Date: Wednesday, January 21, 2015				Sheet	28	of 102

Main Func = Audio

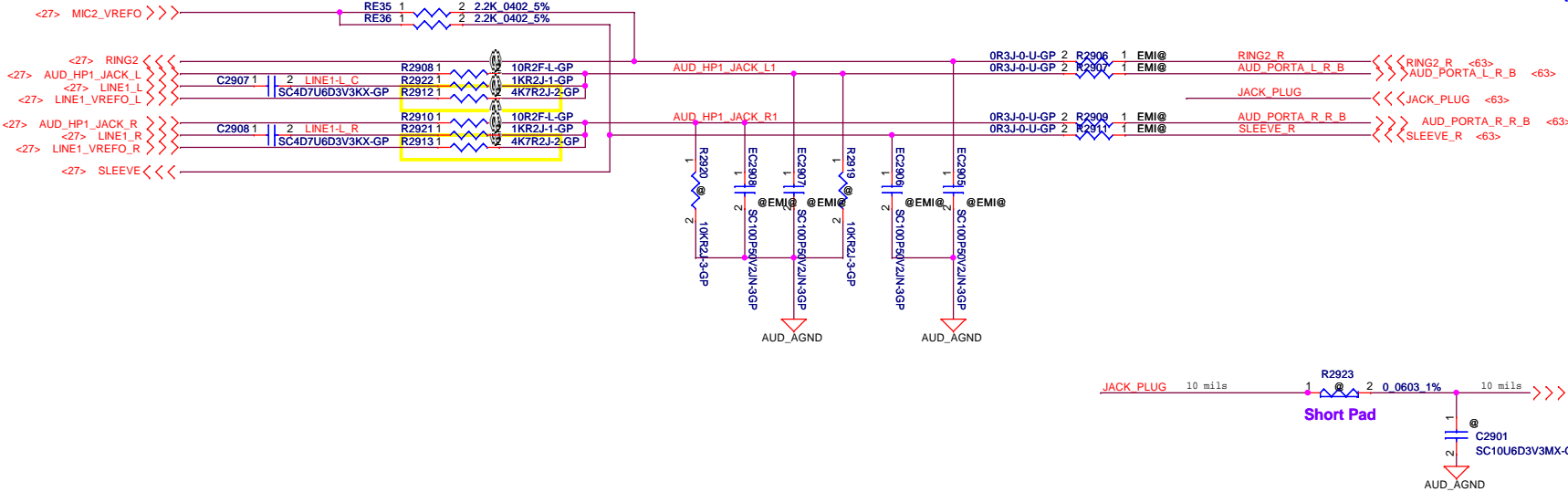
Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

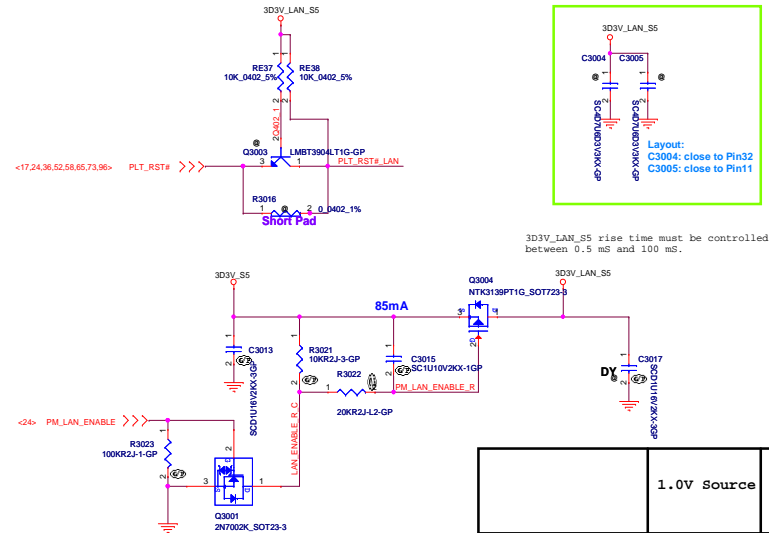
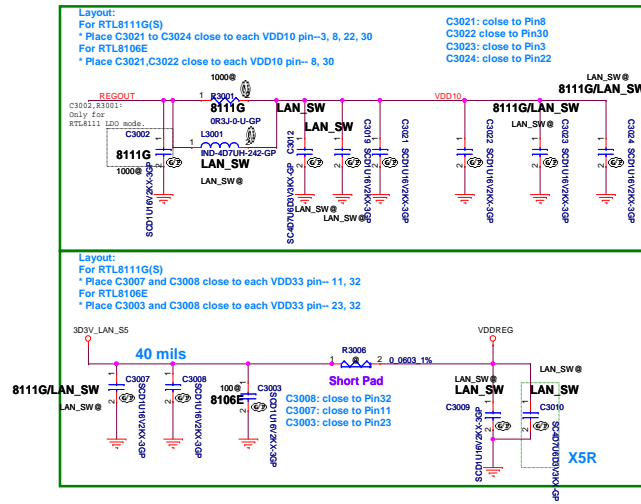


Universal Jack (Moved to I/O Board)

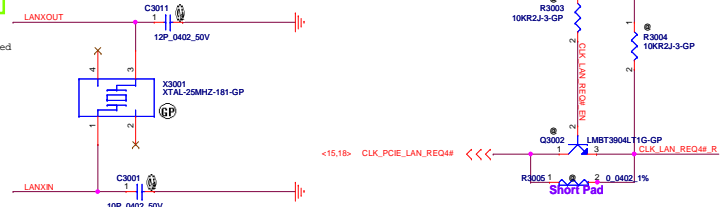
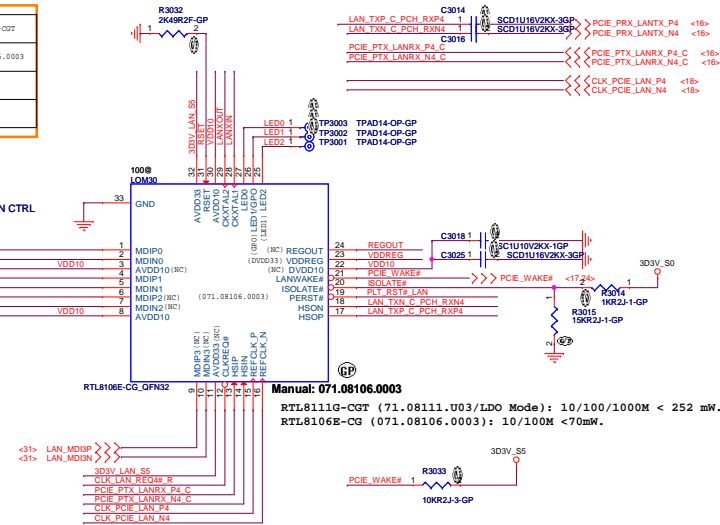
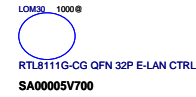


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**LAN CHIP (10/100/1000M & 10/100M co-lay)**

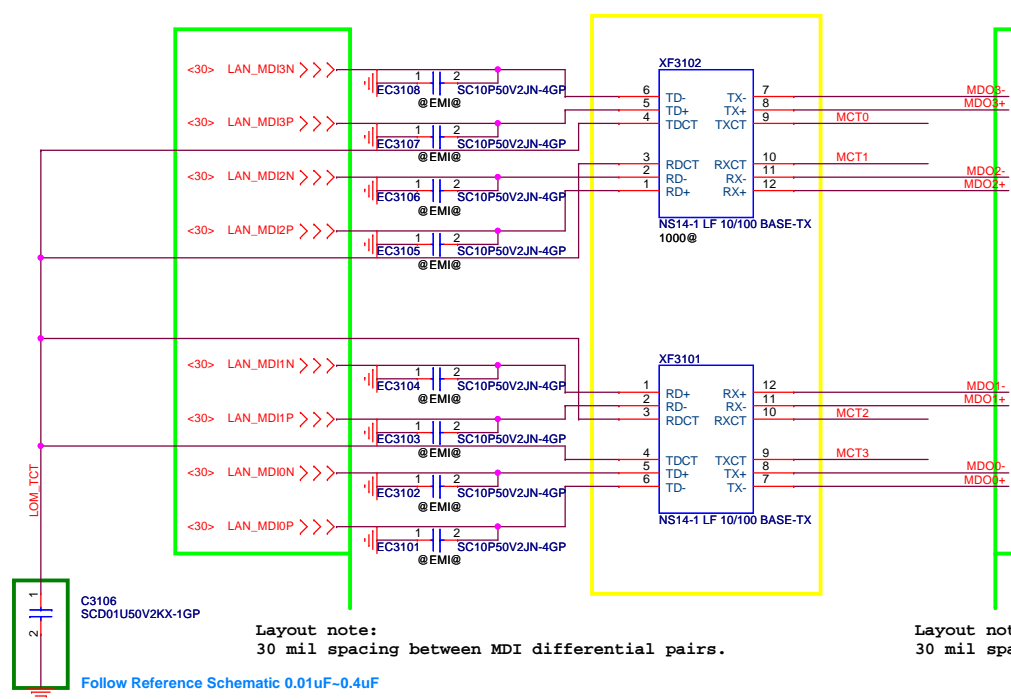


RTL8111GUS-CG	RTL8111G-OUT	RTL8106EUS-CG	RTL8106E-OUT
71.08111.W03	71.08111.U03	71.08106.W03	071.08106.W003
SNR mode	LDO mode	SNR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

[illegible]

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2015/01/20				LAN RTL8106	
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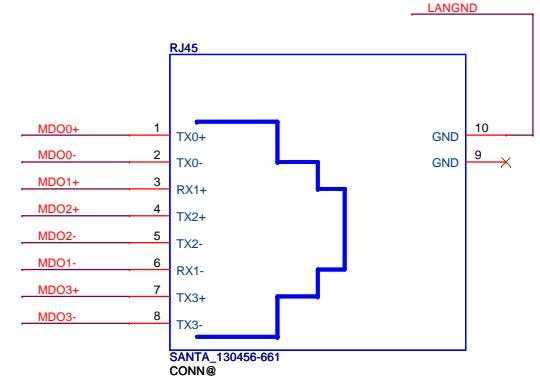
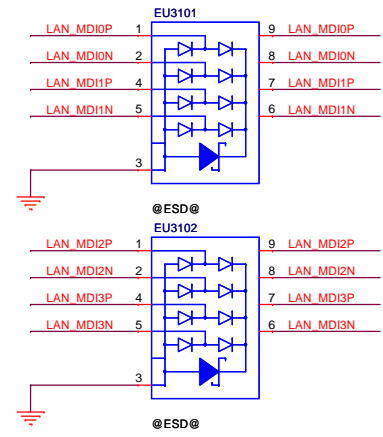
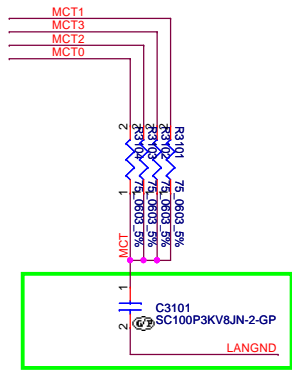
LAN TransFormer (10/100/1000M & 10/100M co-lay)



Layout note:  
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF

Layout note:  
30 mil spacing between MDI differential pairs.



A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.

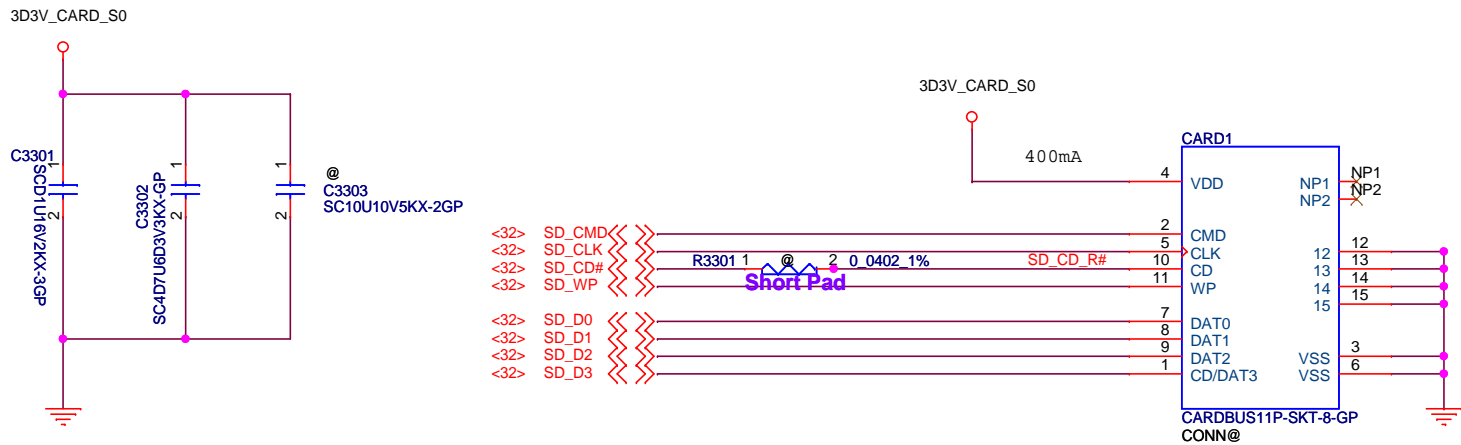
A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.



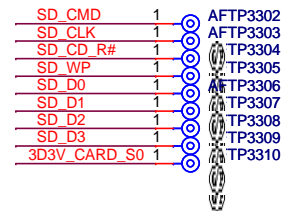
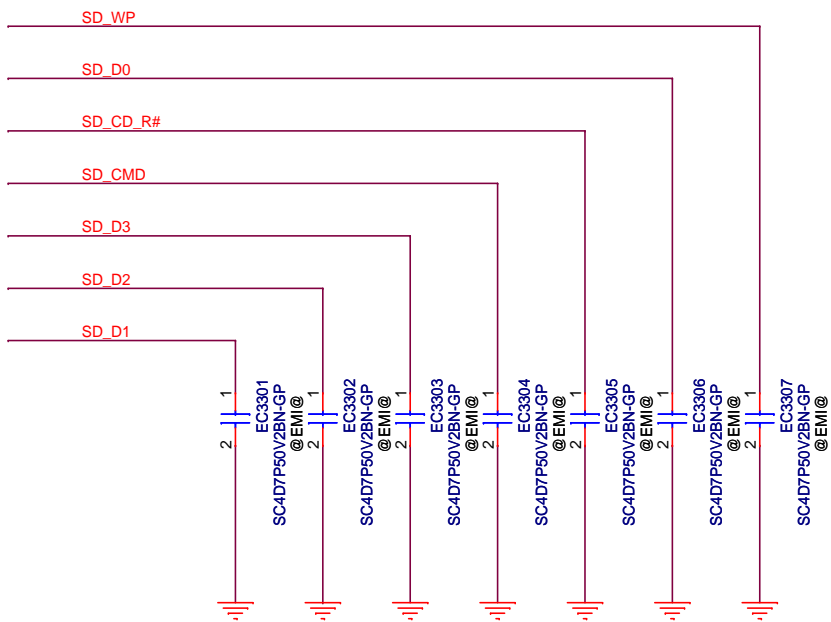
A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.



# Main Func = Card Reader



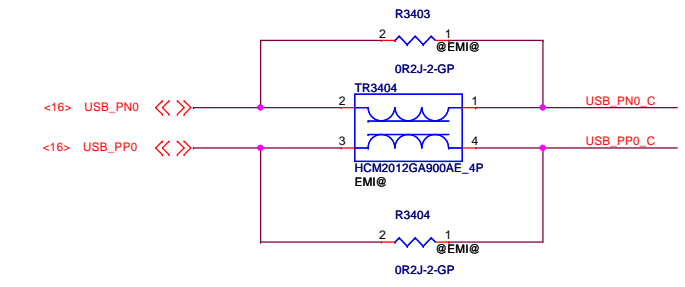
## For EMI Reserved



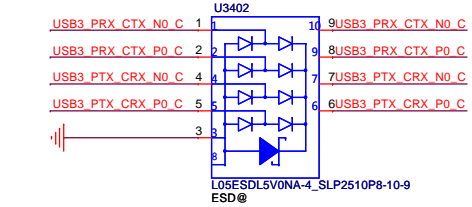
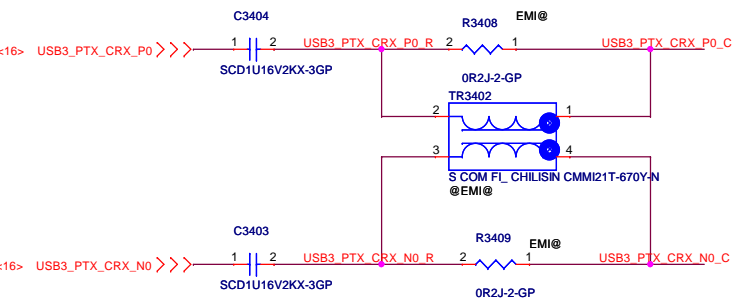
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Size		Document Number			Rev
		LA-B483P			A00
Date:		Wednesday, January 21, 2015		Sheet	33 of 102

Main Func = USB3.0 Port1

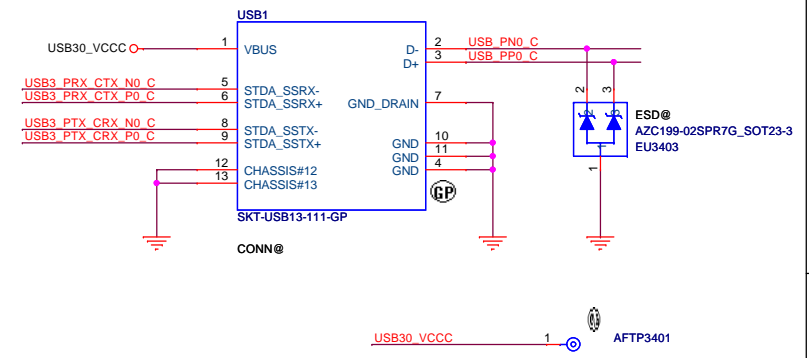
USB2.0 Port2 and USB2.0 Port3 are on IOBD



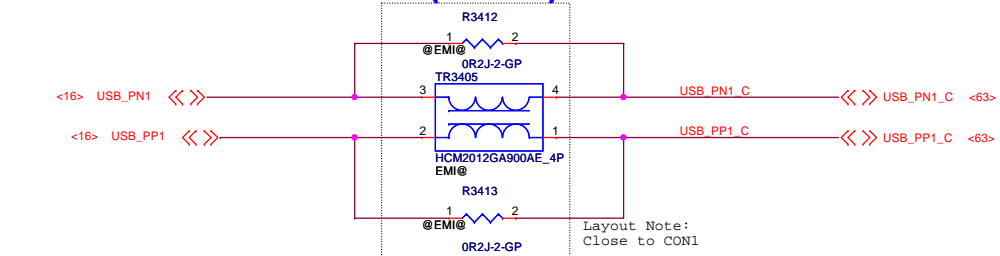
USB2.0/3.0 filter use SM070003Q00



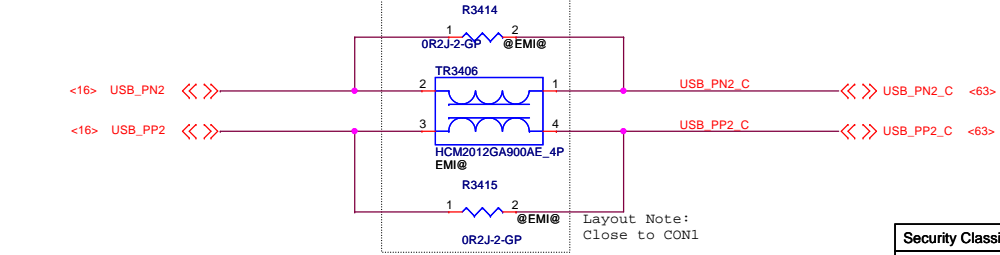
USB3.0 Port1



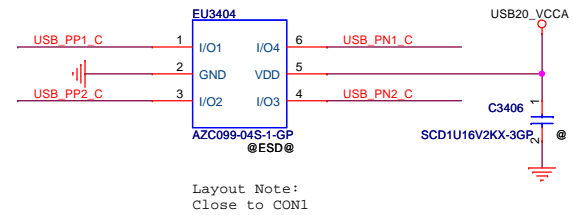
USB2 (USB2.0) CMC



USB3 (USB2.0) CMC

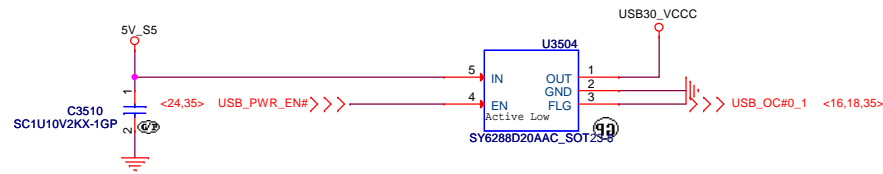


USB ESD Diode



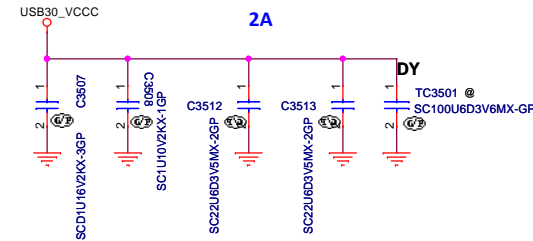
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title	USB3.0 CONN
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				Rev	A00

## Main Func = USB3.0 Port1



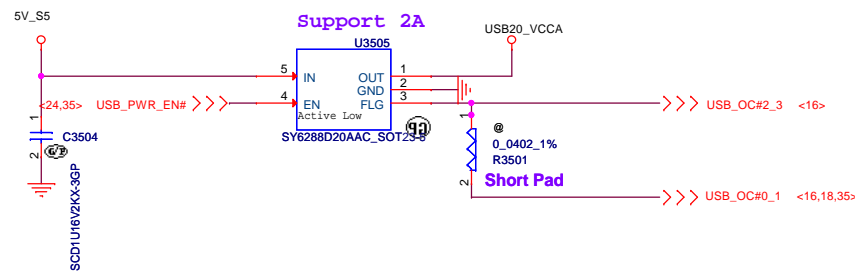
## USB3.0 Port1

Layout Note: Close USB1



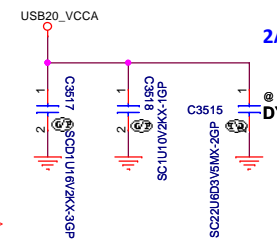
## Main Func = USB2.0 Port2

## Main Func = USB2.0 Port3



## USB2.0 Port3 (IO Board)

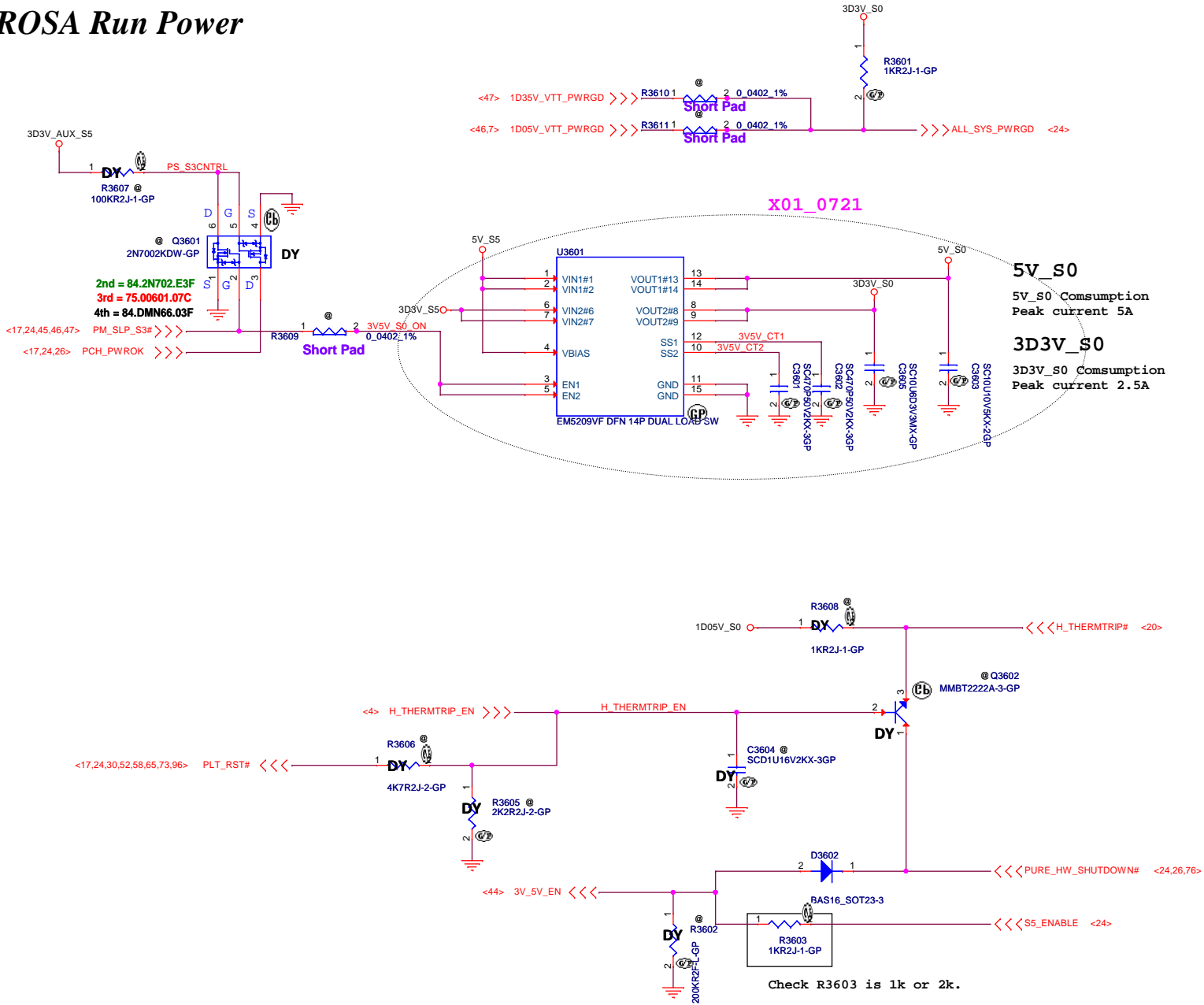
Layout Note: Close CON1



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				Date	Wednesday, January 21, 2015
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				Rev	A00

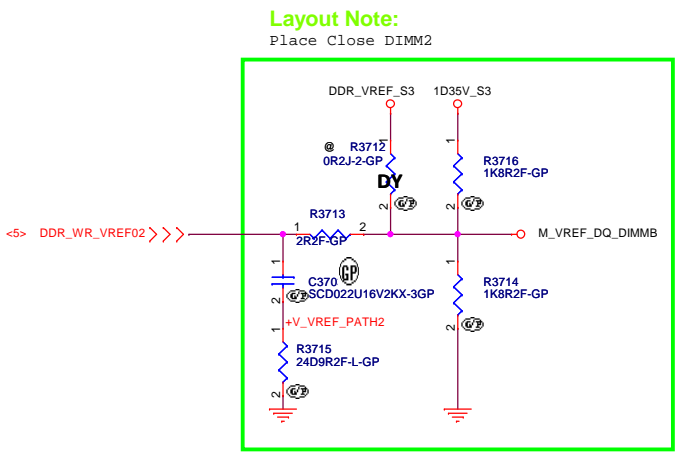
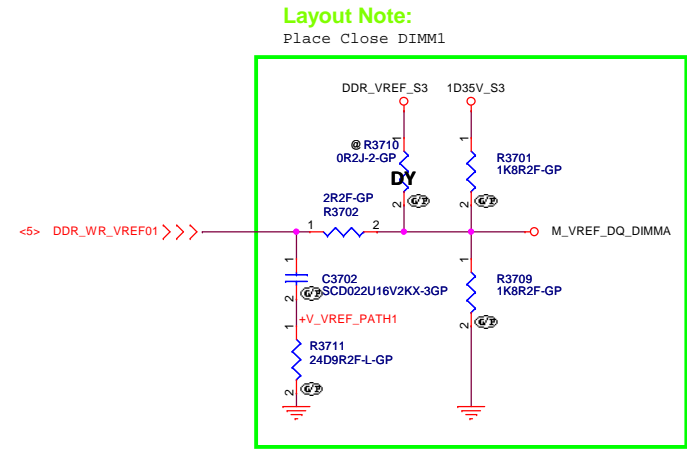
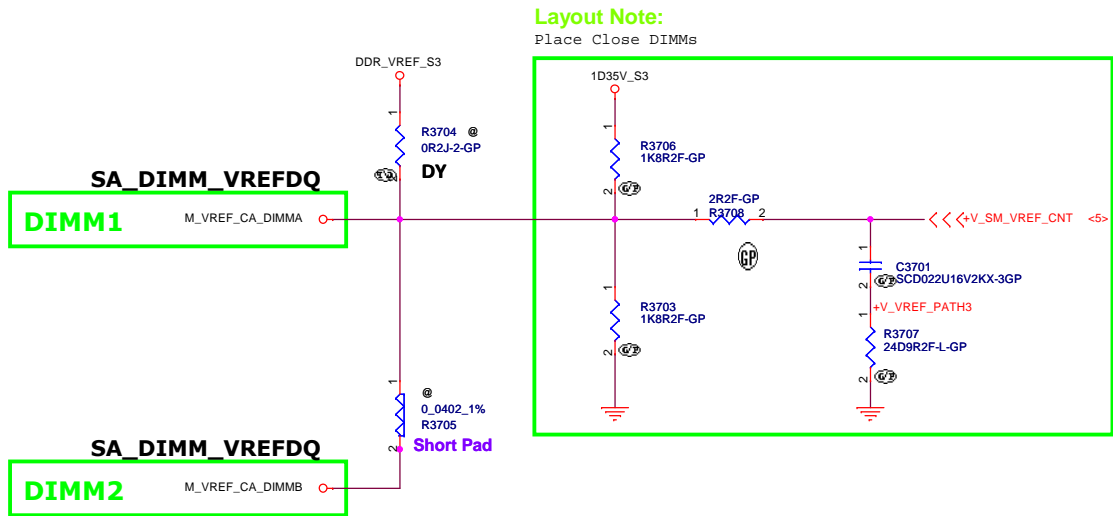
Power Good

ROSA Run Power

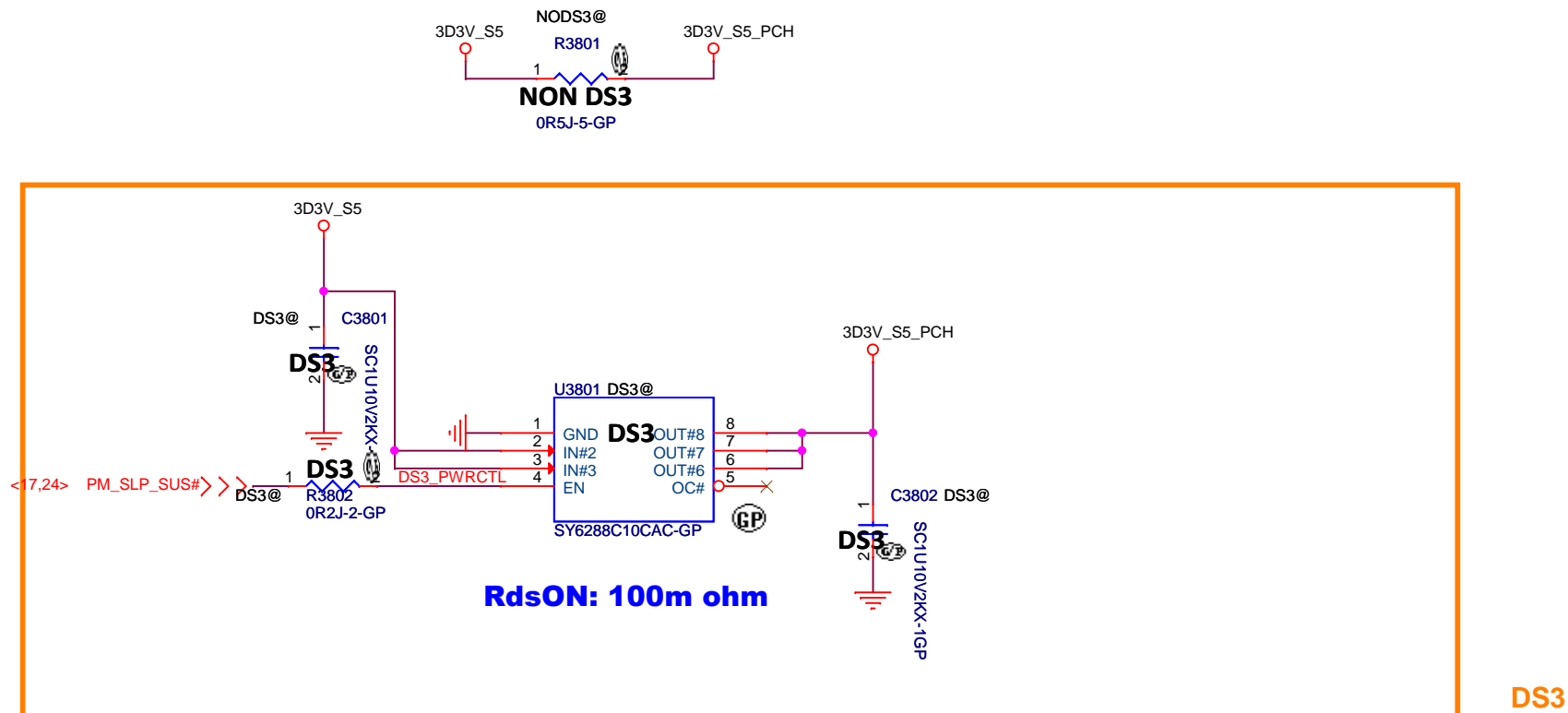


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Main Func = DIMM1  
Main Func = DIMM2



## Main Func = Power Plane & Sequence



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				Document Number				Rev		
				LA-B483P				A00		
				Date:	Wednesday, January 21, 2015		Sheet	38	of	102

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						Document Number		Rev	
						LA-B483P		A00	
						Date:		Wednesday, January 21, 2015	

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				Document Number	Rev	
				LA-B483P	A00	
				Date:	Wednesday, January 21, 2015	Sheet 40 of 102

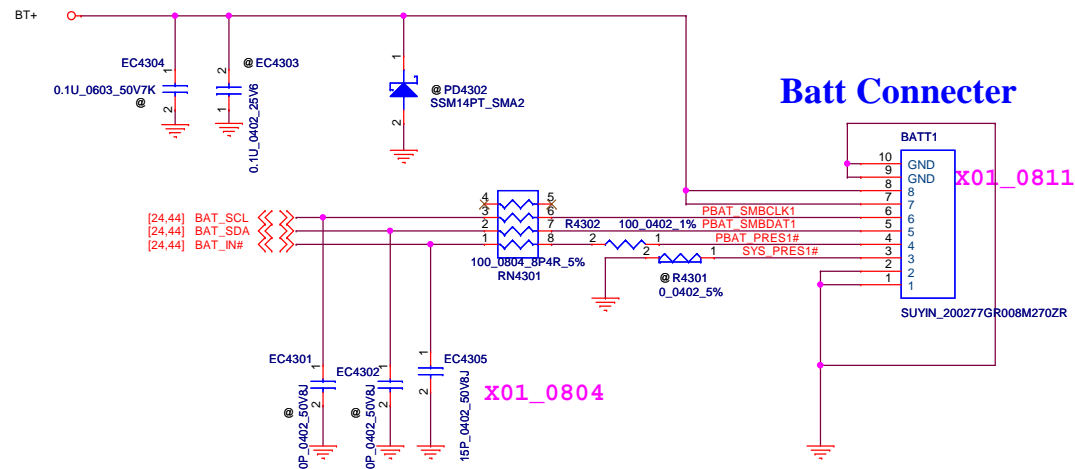


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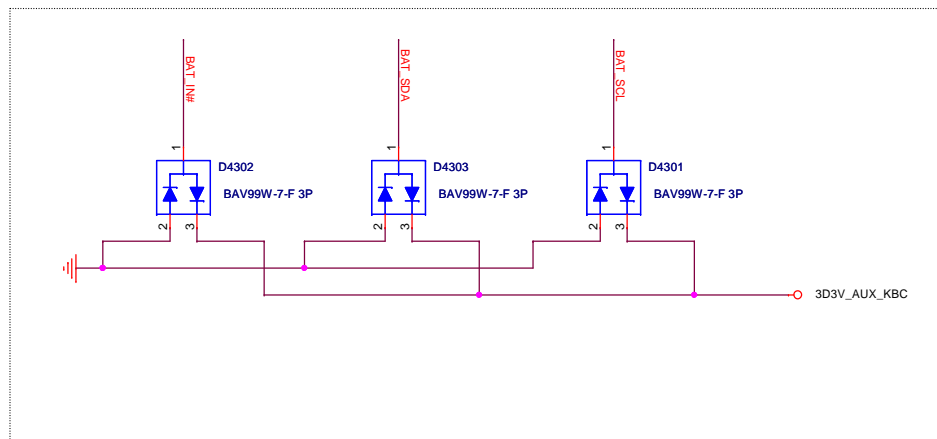
Security Classification		Compal Secret Data				<b>Compal Electronics, Inc.</b>					
Issued Date		2015/01/20		Deciphered Date		2015/12/31		Title			
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						Size		Document Number		Rev	
								<b>LA-B483P</b>		A00	
						Date:		Wednesday, January 21, 2015		Sheet 41 of 102	



Main Func = M-BAT Input

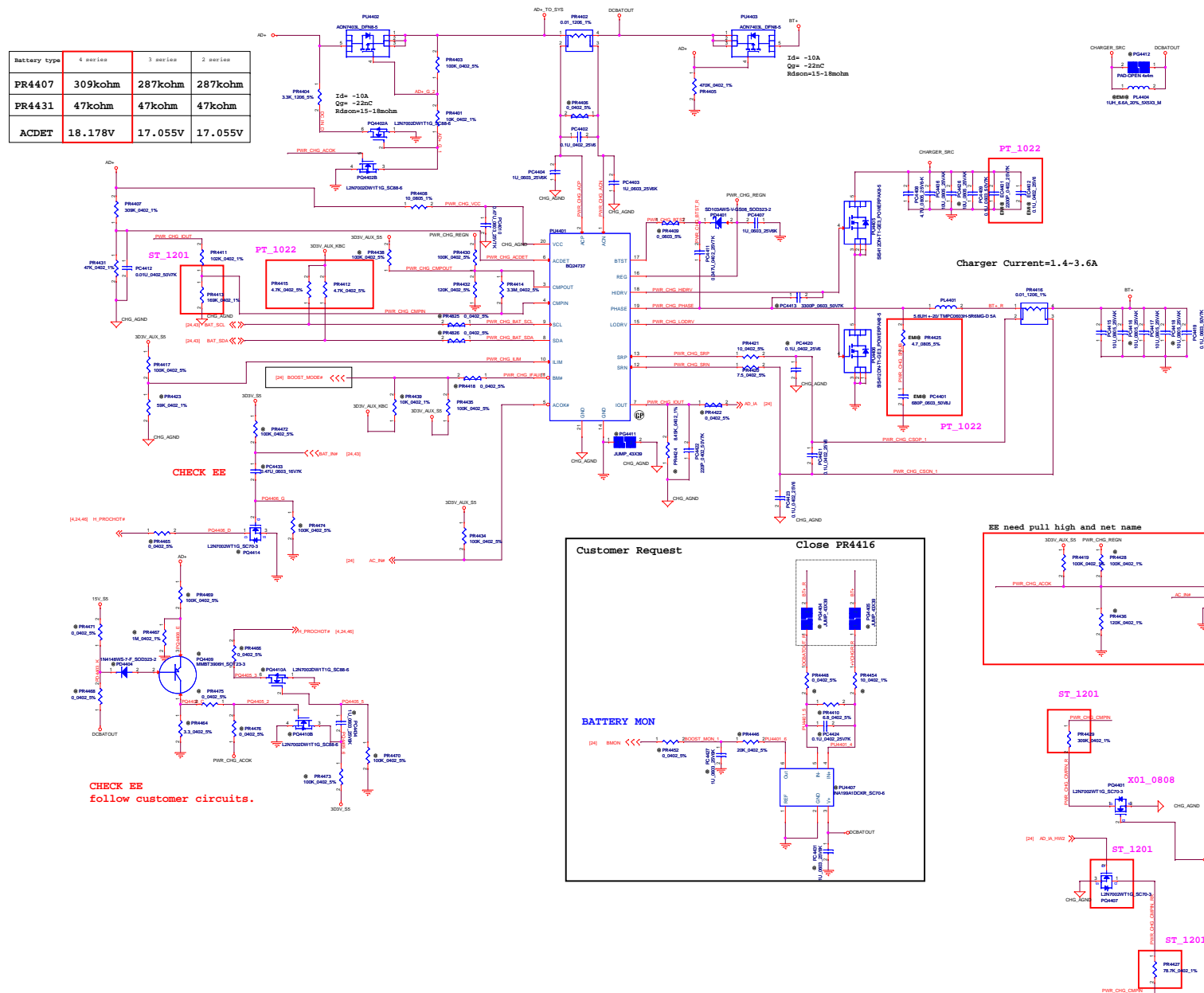


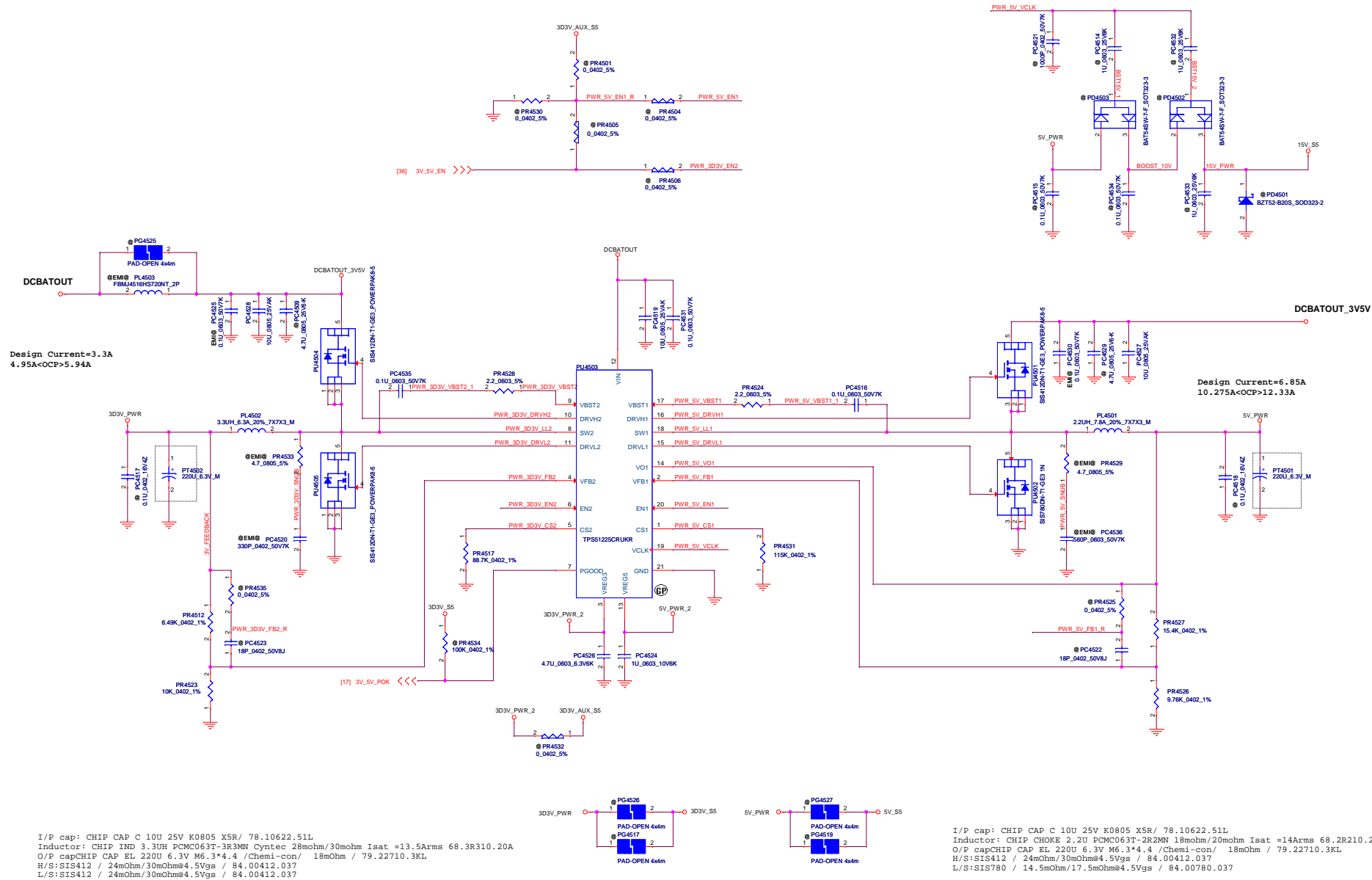
Placement: Close to Batt Connector



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title <b>BATT CONN</b>	
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Date: Wednesday, January 21, 2015				Sheet 43	of 102

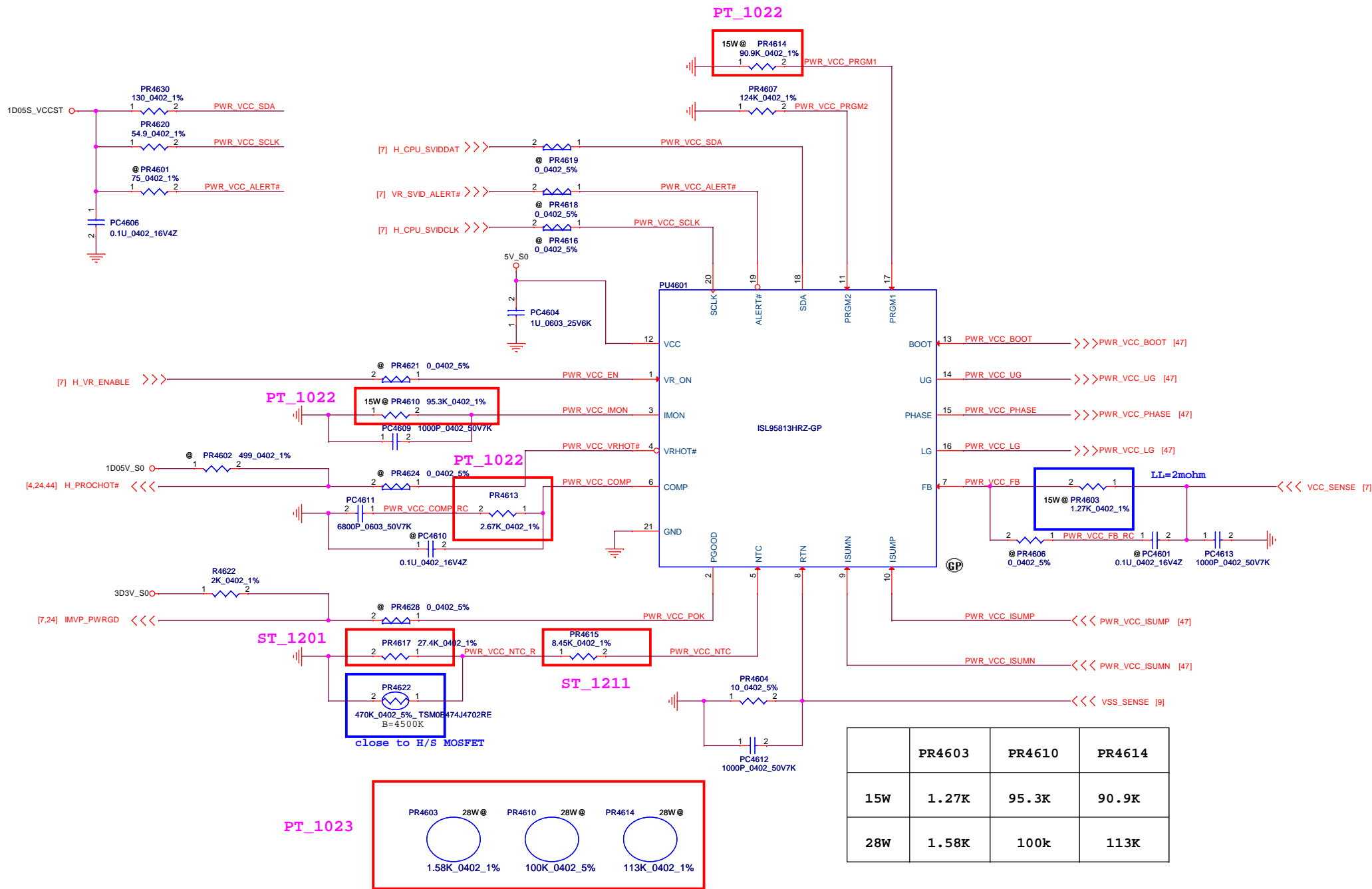
Battery type	4 series	3 series	2 series
PR4407	309kohm	287kohm	287kohm
PR4431	47kohm	47kohm	47kohm
ACDET	18.178V	17.055V	17.055V





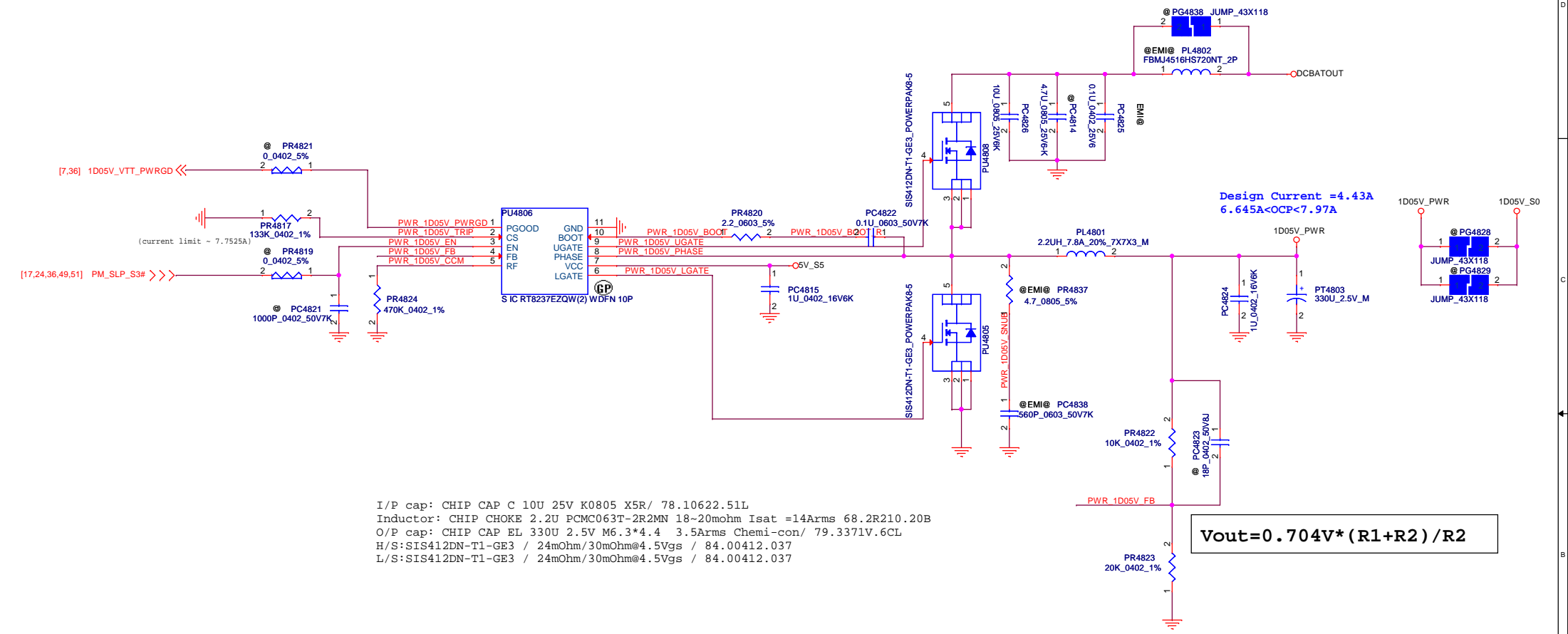
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title	TPS51225_5V/3D3V
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number <b>LA-B483P</b>
				Date	Wadeyuan January 21, 2015
				Sheet	46 of 102
				Rev	A00

Main Func = CPU\_CORE



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Main Func = 1D05V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B  
O/P cap: CHIP CAP EL 330U 2.5V M6.3\*4.4 3.5Arms Chemi-con/ 79.3371V.6CL  
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$

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Size		Document Number		Rev	
LA-B483P		A00		Date: Wednesday, January 21, 2015	
Sheet		48		of 102	

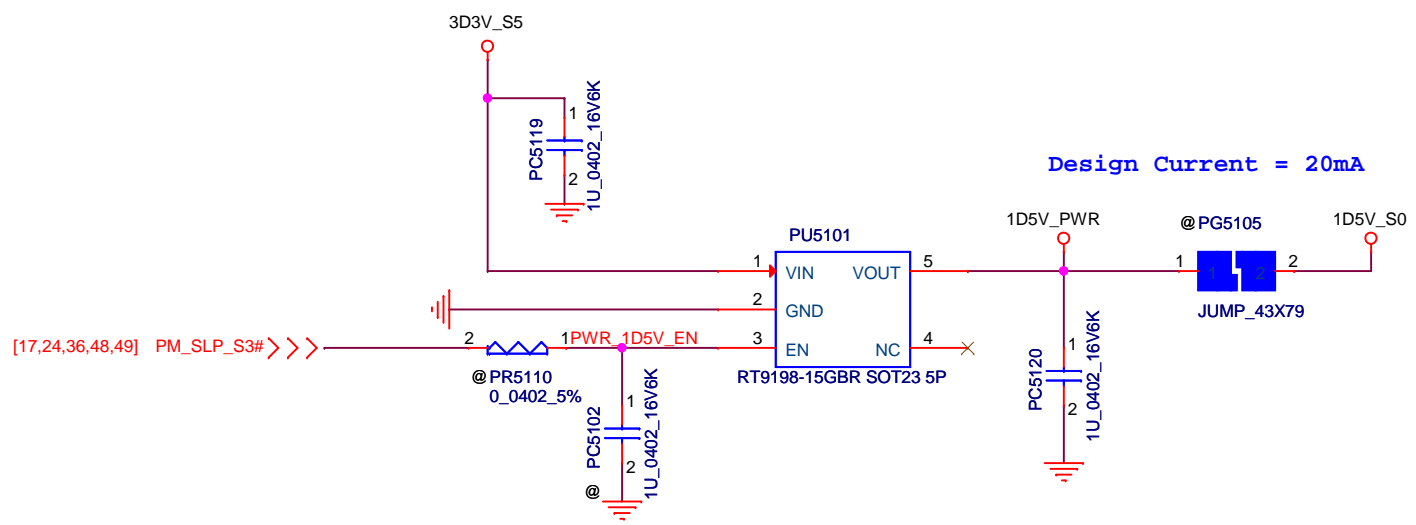




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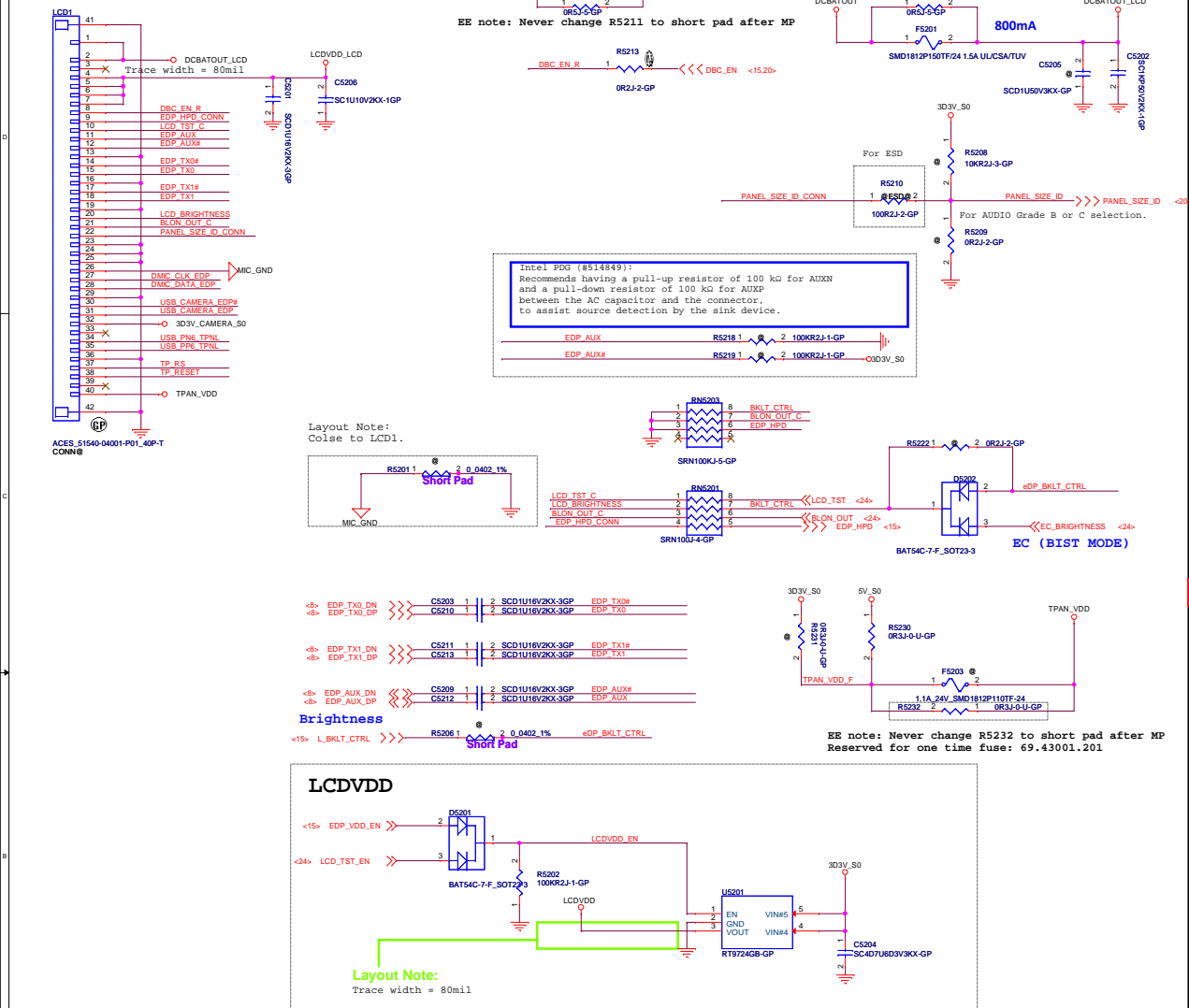
Security Classification		Compal Secret Data				Compal Electronics, Inc.						
Issued Date		2015/01/20		Deciphered Date		2015/12/31		Title				
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						Size		Document Number			Rev	
								LA-B483P			A00	
						Date:		Wednesday, January 21, 2015		Sheet		50 of 102

Main Func = 1D5V

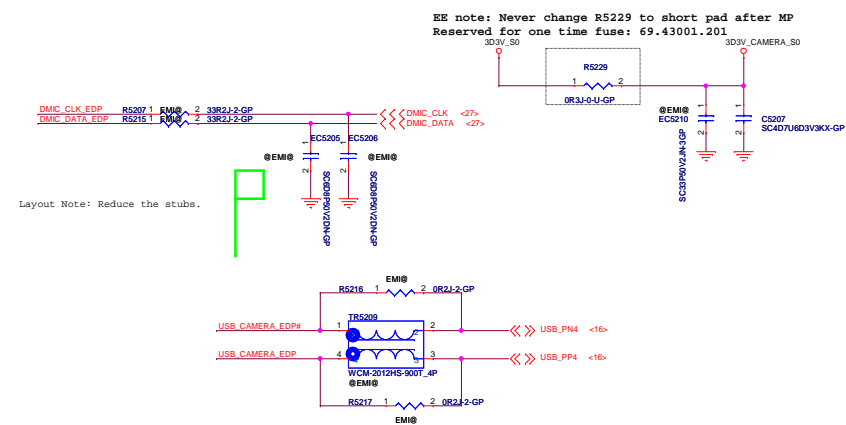


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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title	TLV70215 1D5V	
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				Document Number	LA-B483P	
Date: Wednesday, January 21, 2015				Sheet	51	of 102

# Main Func = LCD

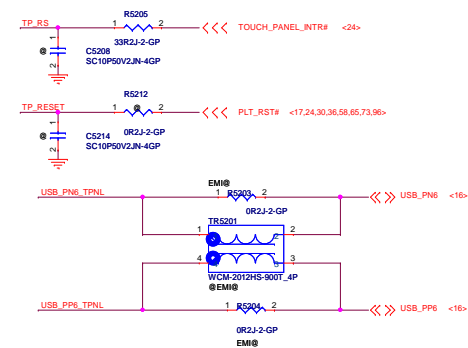


# Main Func = CAM



# Main Func = TS

## Touch Panel

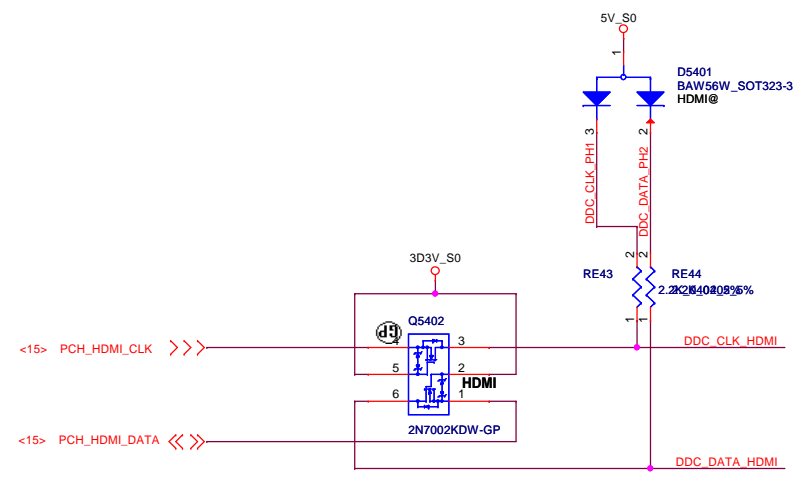
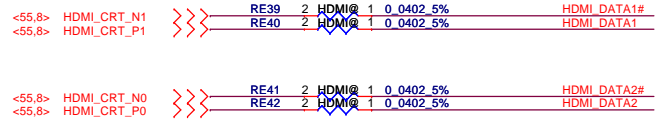
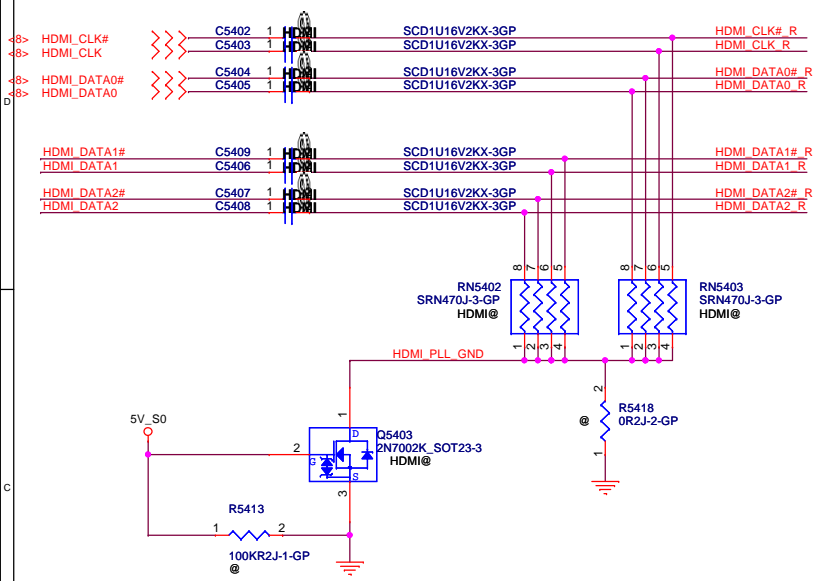


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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title	
				LCD/Inverter CONN	
				Size	Document Number
				LA-B483P	
				Date	Thursday, January 22, 2015
				Sheet	52 of 102

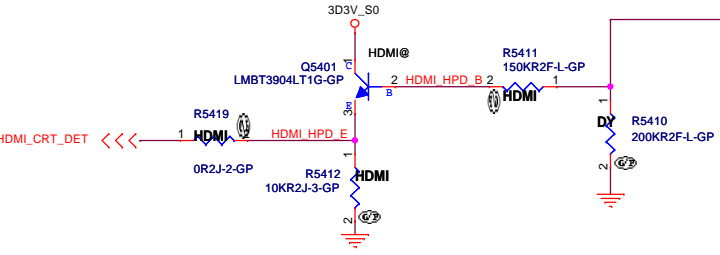
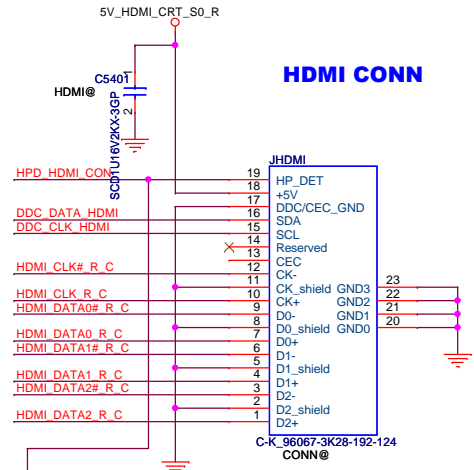
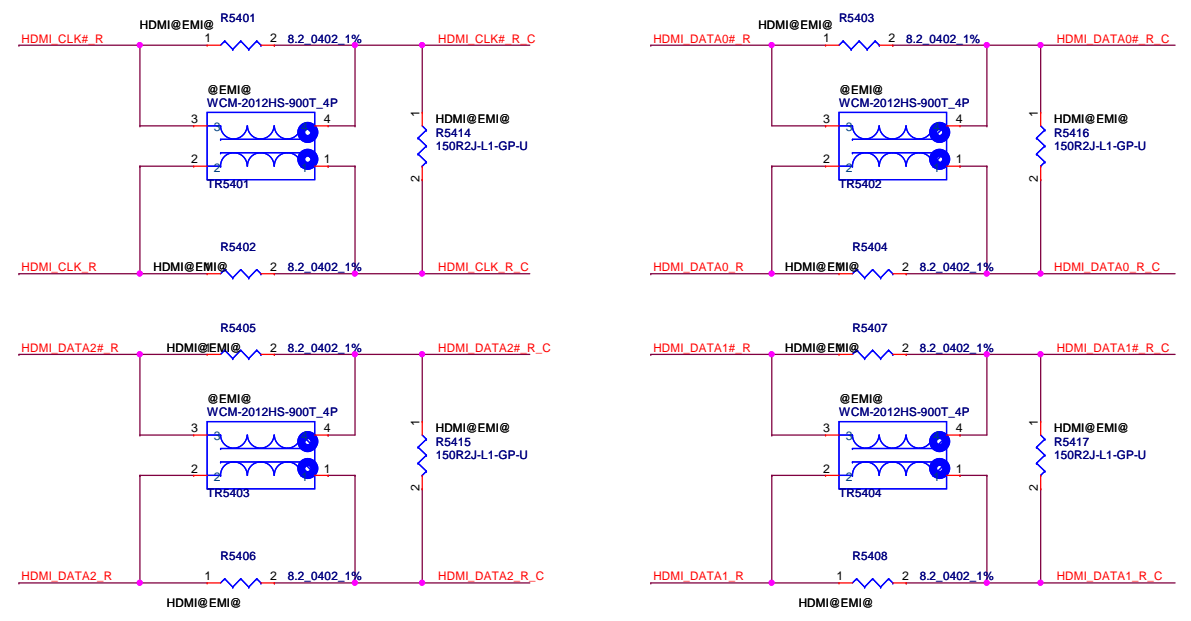
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					LA-B483P	A00
				Date:	Wednesday, January 21, 2015	Sheet 53 of 102

Main Func = HDMI

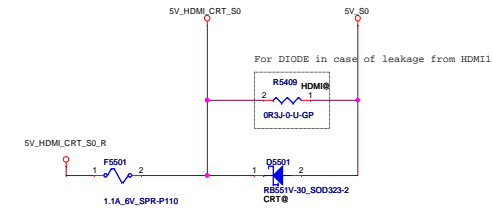
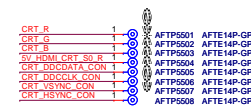
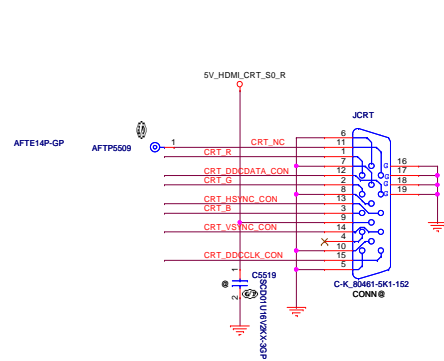


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3rd = 75.00601.07C  
4th = 84.DMN66.03F

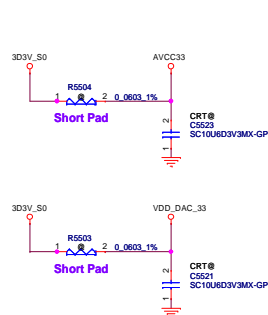
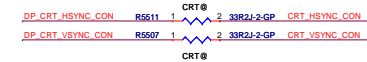
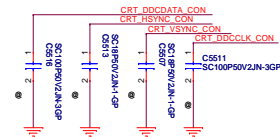
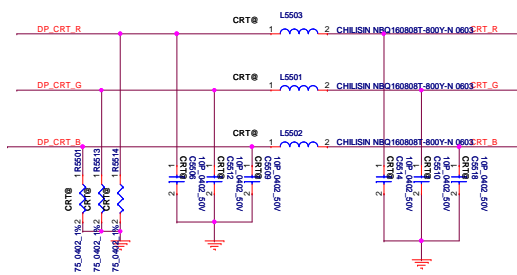


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Deciphered Date				2015/12/31				HDMI L.Shifter/Conn			
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								LA-B483P			
								Date: Wednesday, January 21, 2015			
								Sheet 54 of 102			

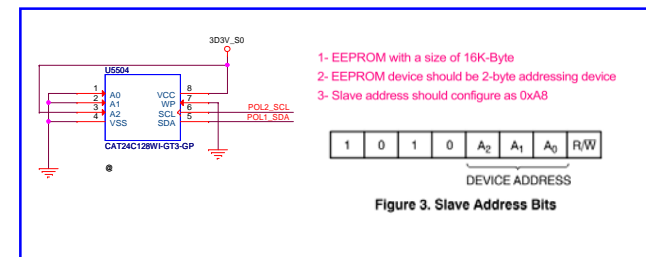
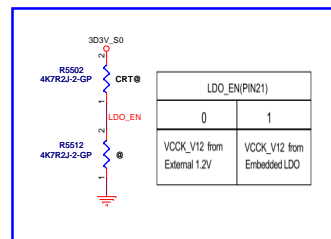
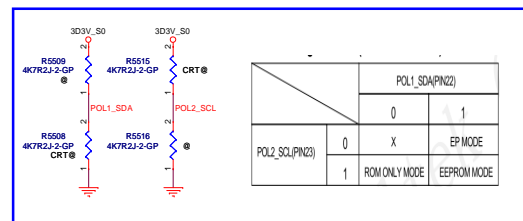
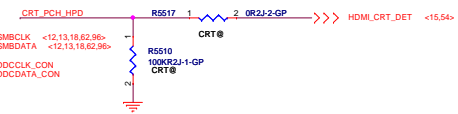
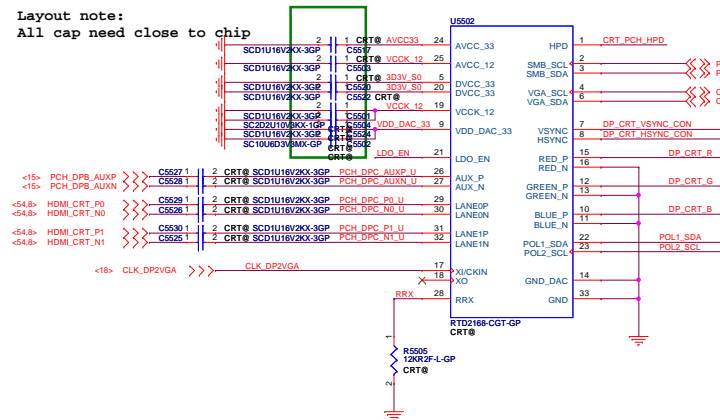
- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8



**CRT RGB**  
**CRT H/VSYNC**  
**CRT SMBUS**



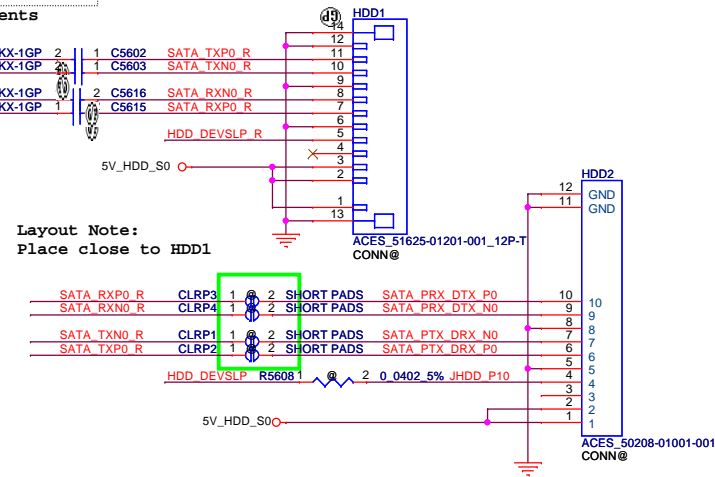
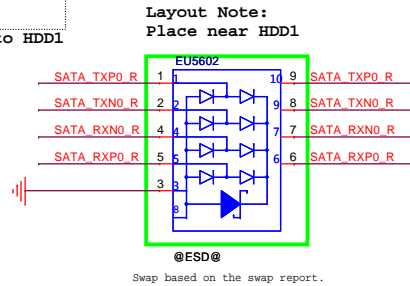
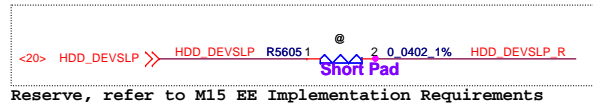
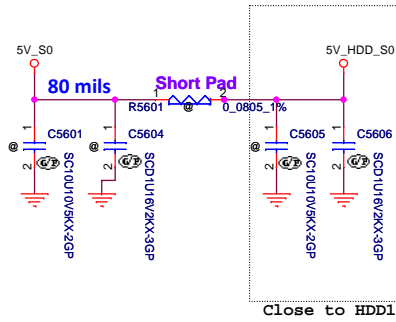
Layout note:  
All cap need close to chip



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Main Func = HDD

## SATA HDD Connector

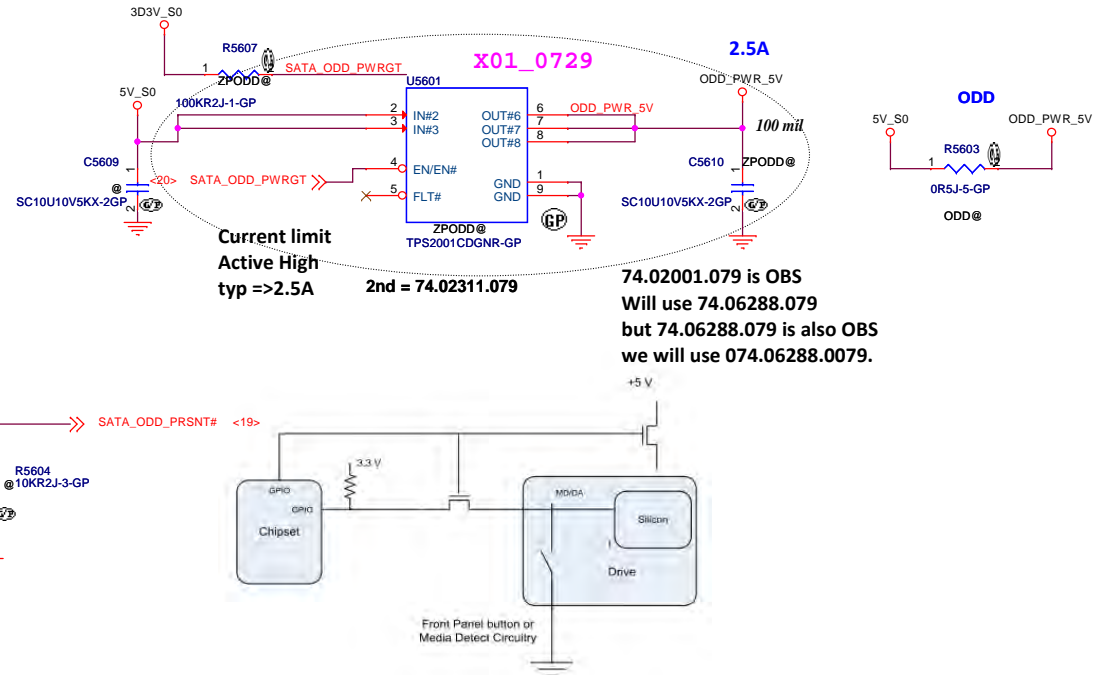
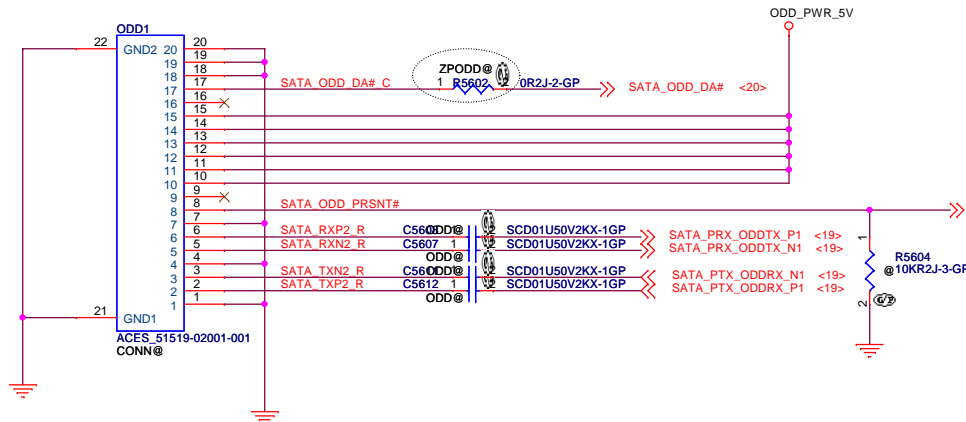


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

## SATA Zero Power ODD

## ODD Connector



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				Date	Wednesday, January 21, 2015
				Sheet	56 of 102
				Rev	A00

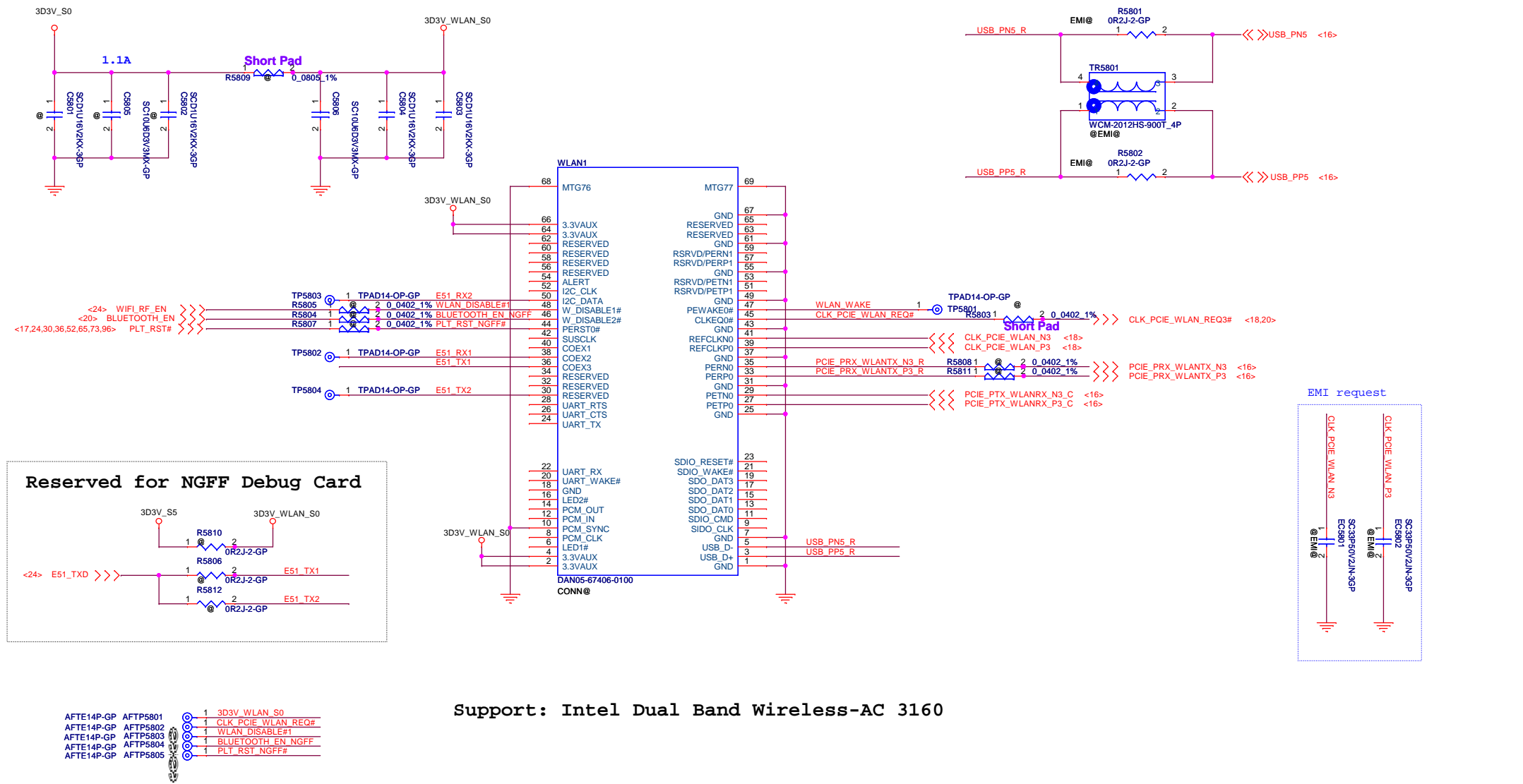


SSID = ESATA

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Main Func = WLAN



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					NGFF WLAN CONN
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			LA-B483P		
		Date	Wednesday, January 21, 2015	Sheet	58 of 102

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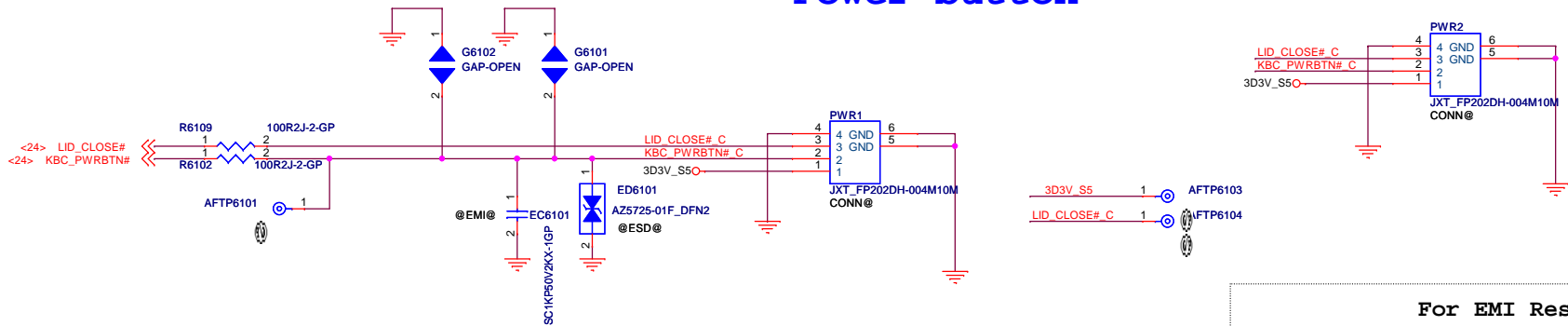
Security Classification		Compal Secret Data				<i>Compal Electronics, Inc.</i>			
Issued Date		2015/01/20		Deciphered Date		2015/12/31		Title	
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						Document Number		Rev	
						<i>LA-B483P</i>		A00	
						Date:		Wednesday, January 21, 2015	

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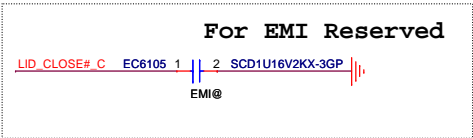
Security Classification		Compal Secret Data				Compal Electronics, Inc.									
Issued Date		2015/01/20		Deciphered Date		2015/12/31		Title							
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								Team Size		Document Number				Rev	
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Main Func = Power BTN

Power button



EC6101 must be used 1000pF.



Main Func = Battery LED

Low actived from KBC GPIO

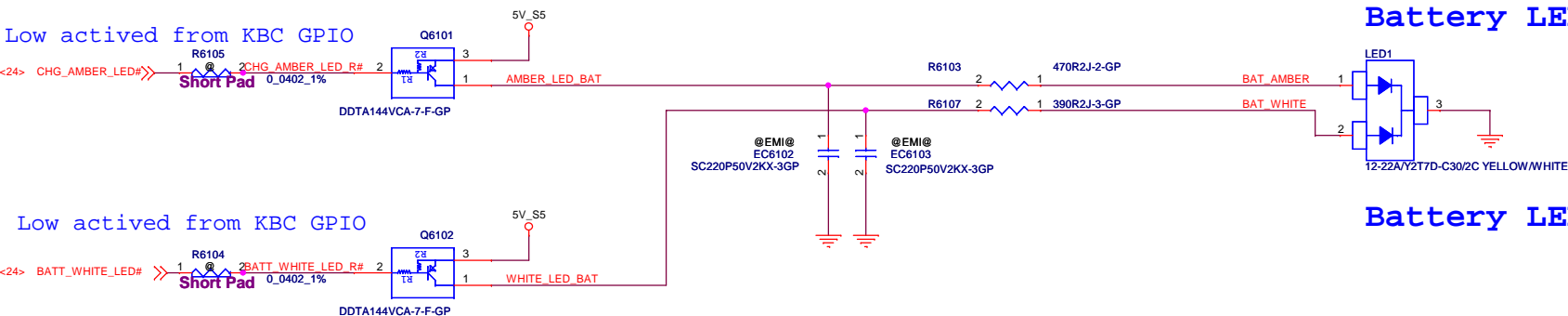
<24> CHG\_AMBER\_LED#

Low actived from KBC GPIO

<24> BATT\_WHITE\_LED#

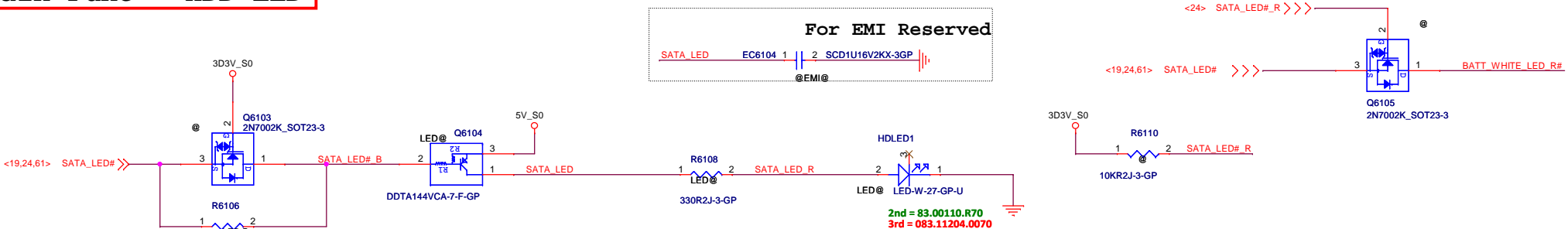
Battery LED1(AMBER\_LED)

Battery LED2 (WHITE\_LED)



Main Func = HDD LED

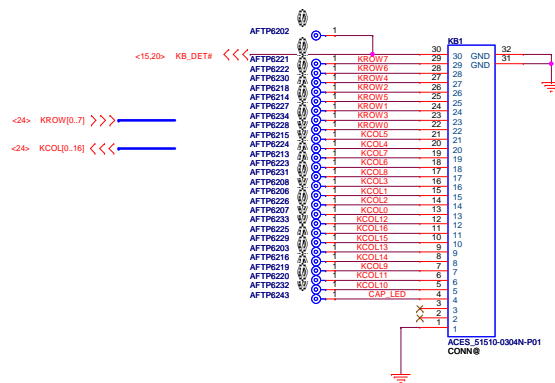
For EMI Reserved



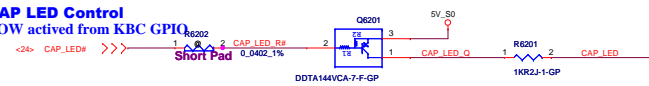
SATA HDD LED  
LOW actived from PCH GPIO

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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								Document Number			
								LA-B483P			
								Date			
								Wednesday, January 21, 2015			
								Sheet			
								61			
								of			
								102			
								Rev			
								A00			

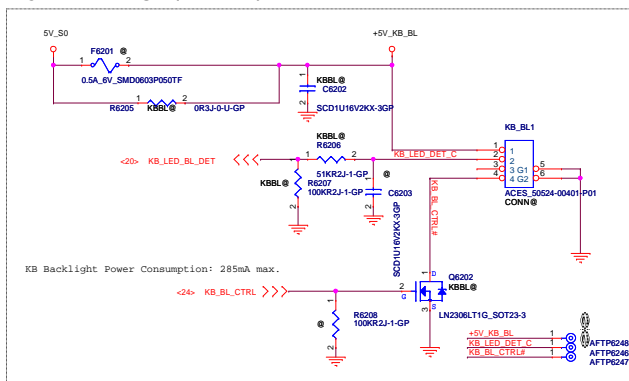
### Internal Keyboard Connector (DVC40)



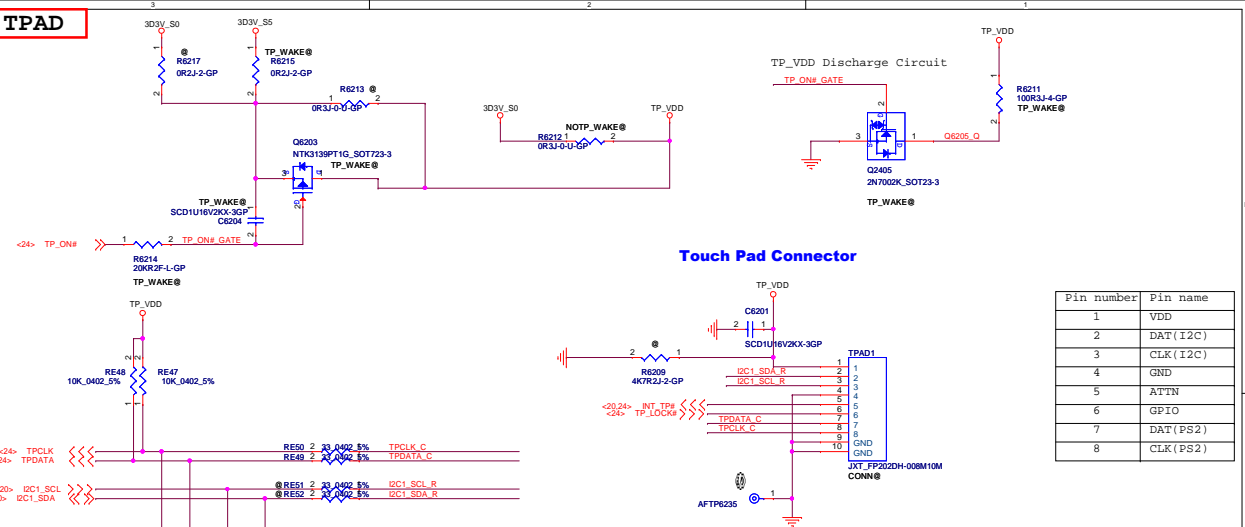
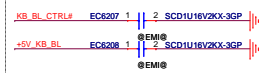
**CAP LED Control**  
LOW actived from KBC GPIO



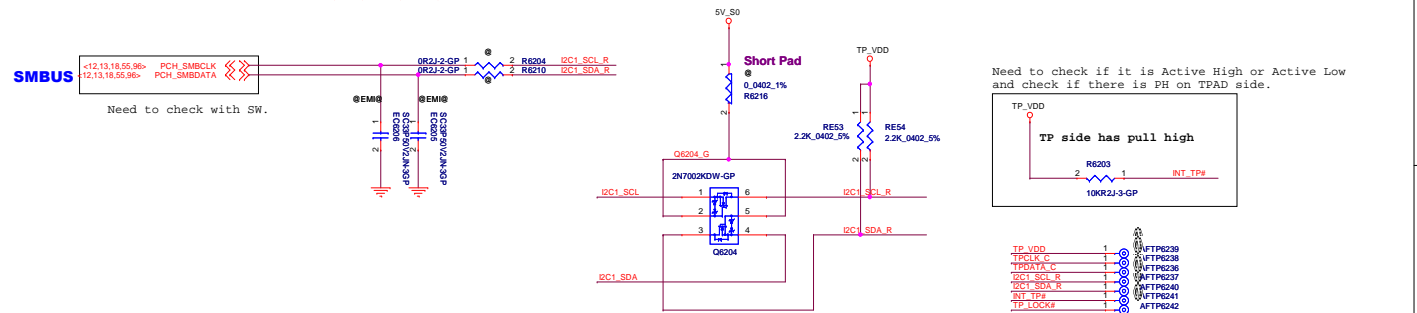
**Keyboard Backlight (Reserved)**



For EMI Reserved



**RN6203 and PTP schematic are BOM option for verify I2C leakage issue.**



Main Func = IO Connector

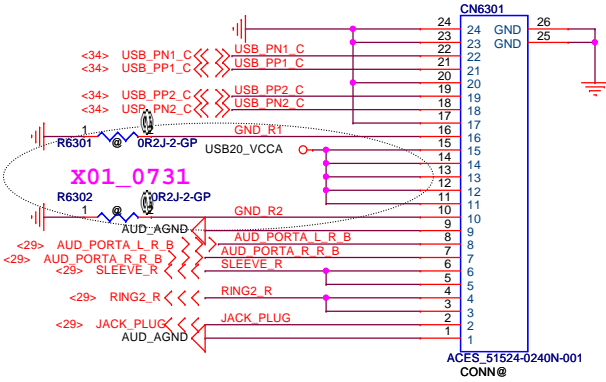
I/O Board Connector

X01\_0808

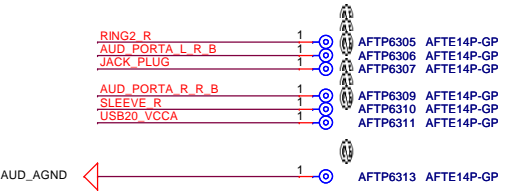
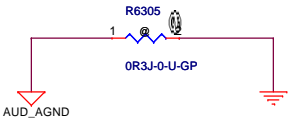
USB2 (USB2.0)  
USB3 (USB2.0)

USB2 (USB2.0)  
USB3 (USB2.0)

Universal Jack



Pitch: 1mm  
Power: 5 pins  
GND: 4 pins  
AGND: 2 Pins



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Main Func = Hall Sensor

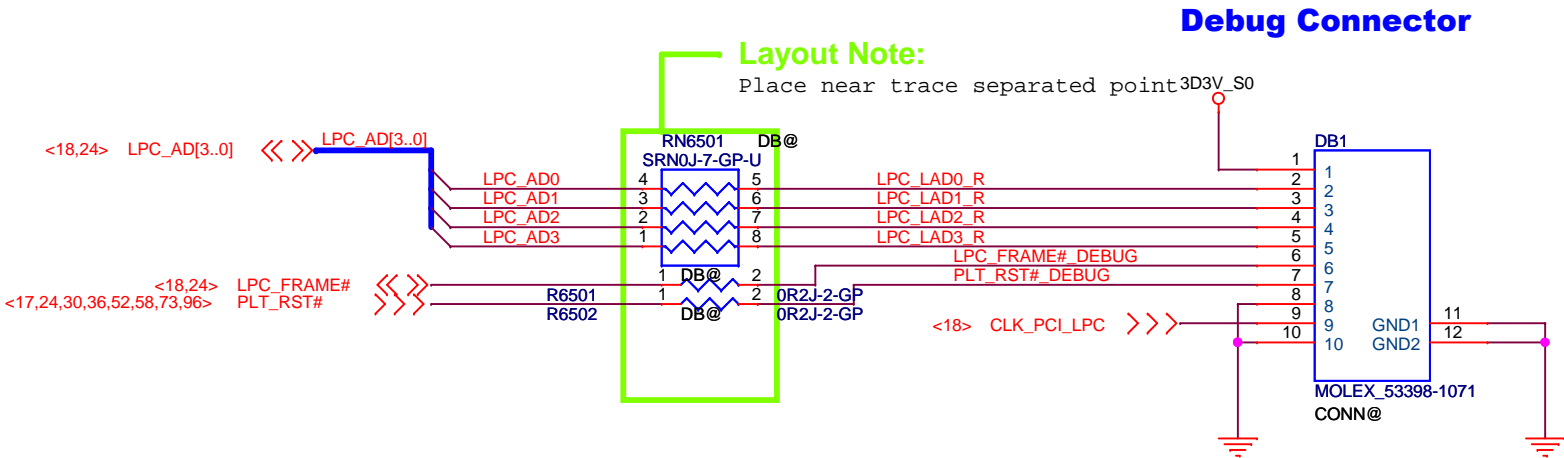
Move to Power Button Board

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Main Func = Debug



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41  
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

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				Document Number	LA-B483P	Rev A00
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## Main Func = dGPU

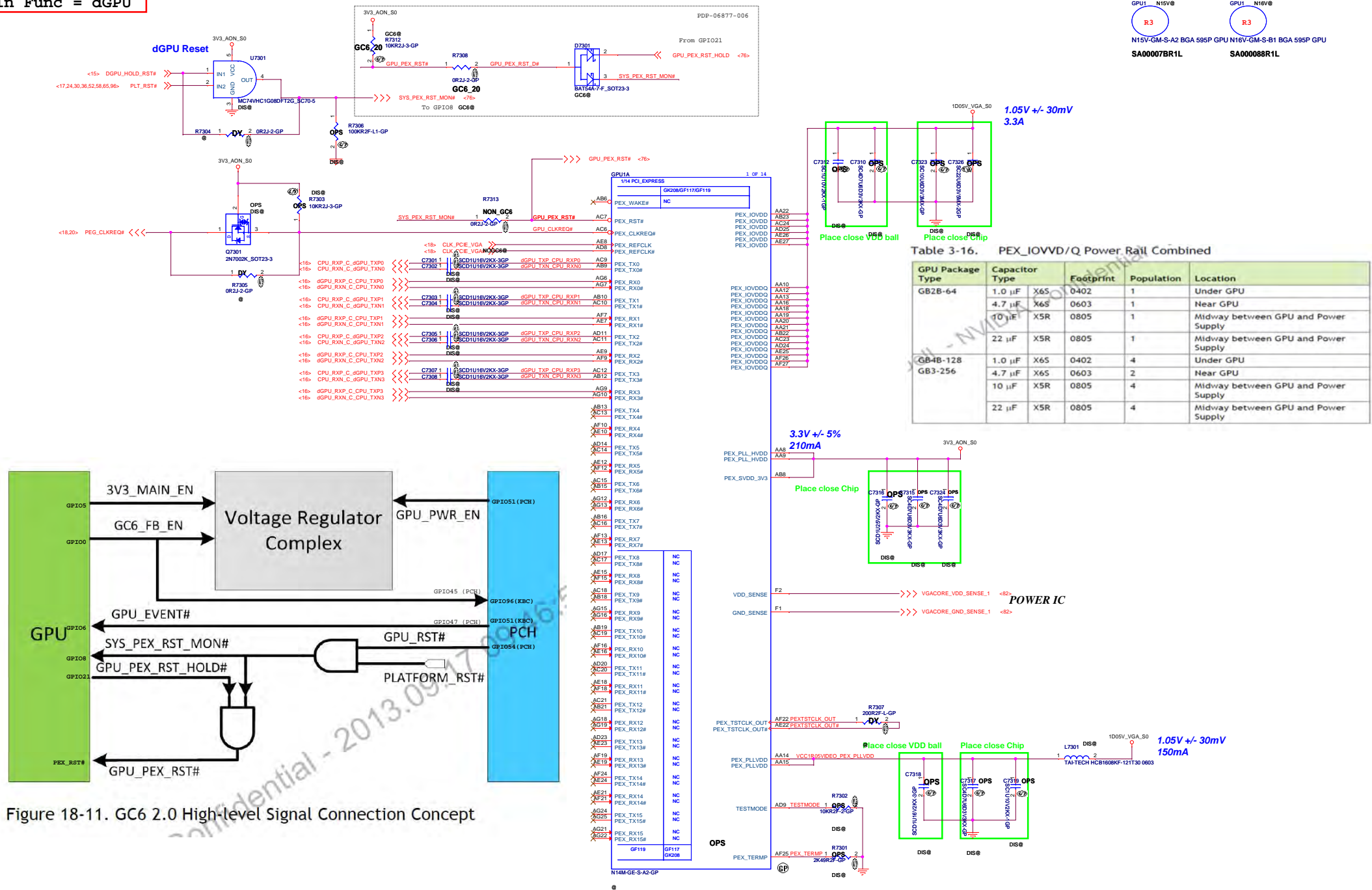


Figure 18-11. GC6 2.0 High-level Signal Connection Concept

N15V-GM-S-A2: JG0YH  
N15S-GT is PXP79

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**OPS**

**OPS**



Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64 DDR3	0.1µF	X7R 0402	2	Under GPU
	1µF	X7R 0603	2	Under GPU
	4.7µF	X6S 0603	2	Under GPU
	10µF	X5R 0805	1	Near GPU
	22µF	X5R 0805	1	Near GPU
GB4B-128 DDR3	0.1µF	X7R 0402	4	Under GPU
	1µF	X7R 0603	4	Under GPU
	4.7µF	X6S 0603	4	Under GPU
	10µF	X5R 0805	2	Near GPU
	22µF	X5R 0805	2	Near GPU

Notes:  
1. The decoupling in this table applies to both single rank and dual rank designs.  
2. If a single partition 64-bit GPU in the GB4B-128 package is used, populate only half of the recommended number of decoupling capacitors of GB4B-128.

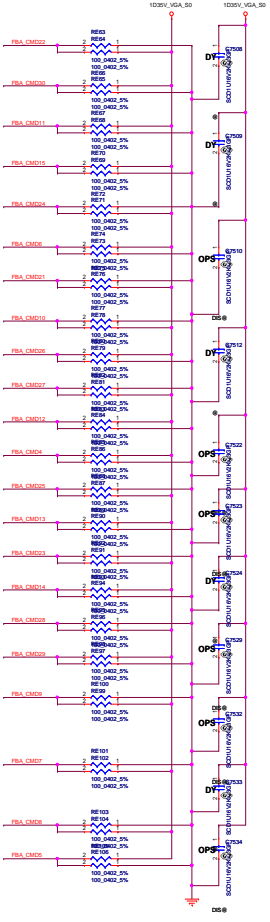
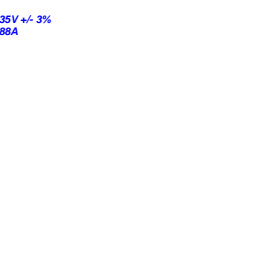
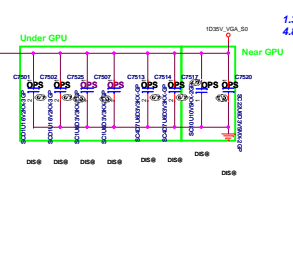
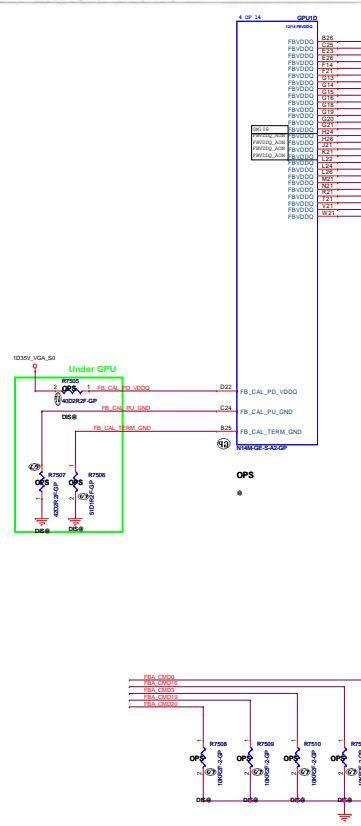
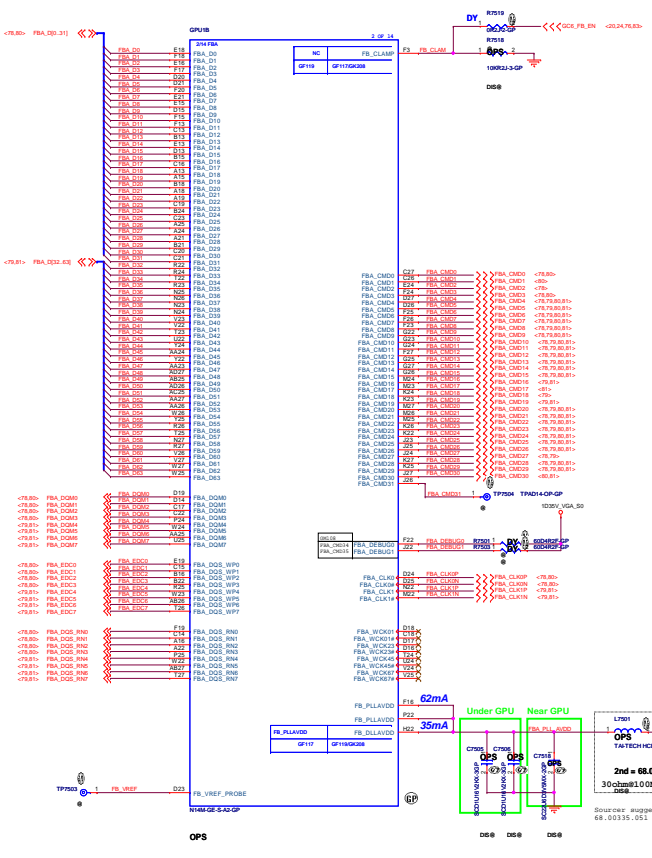


Table 6-4. Mode E Command Mapping

N15x DDR3 Mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1	C51*		C51*	
FBx_CMD2	C50*		C50*	
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	BA5*	BA5*	BA5*	BA5*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16	ODT		ODT	
FBx_CMD17	C51*		C51*	
FBx_CMD18	C50*		C50*	
FBx_CMD19	CKE		CKE	
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE*	WE*
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE*	WE*	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2
FBx_CMD31				
FBx_CMD32				
FBx_CMD33*				

Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

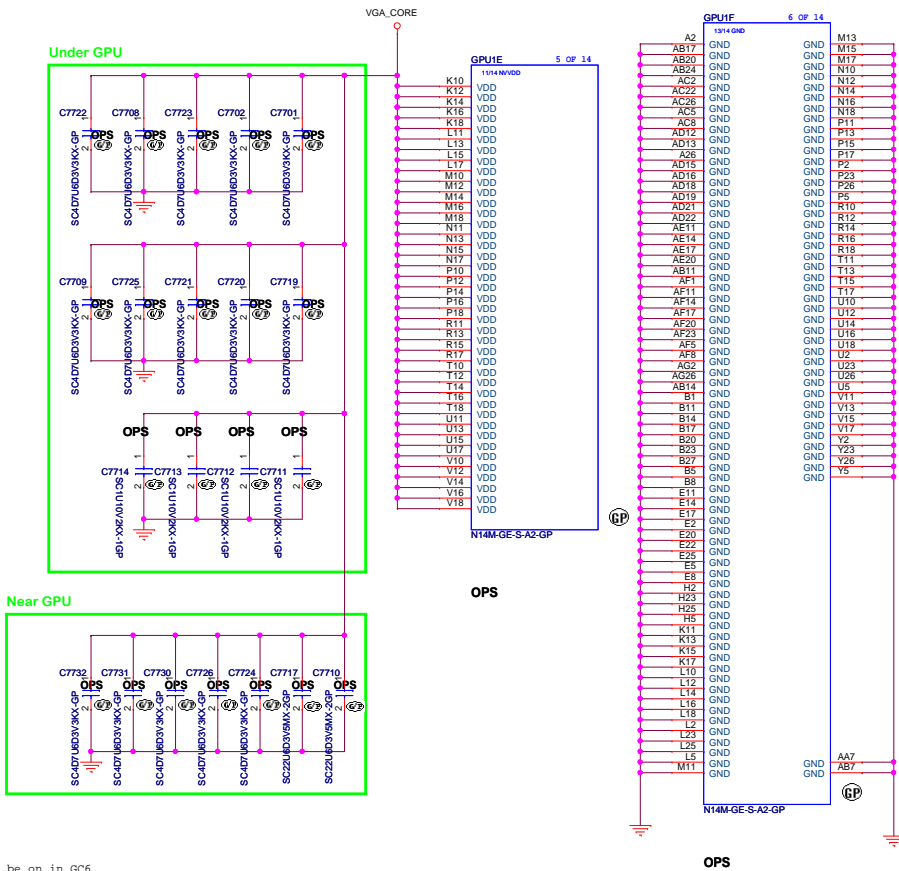
GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64 DDR3	0.1µF	X7R 0402	2	Under GPU
	1µF	X7R 0603	2	Under GPU
	4.7µF	X6S 0603	2	Under GPU
	10µF	X5R 0805	1	Near GPU
	22µF	X5R 0805	1	Near GPU





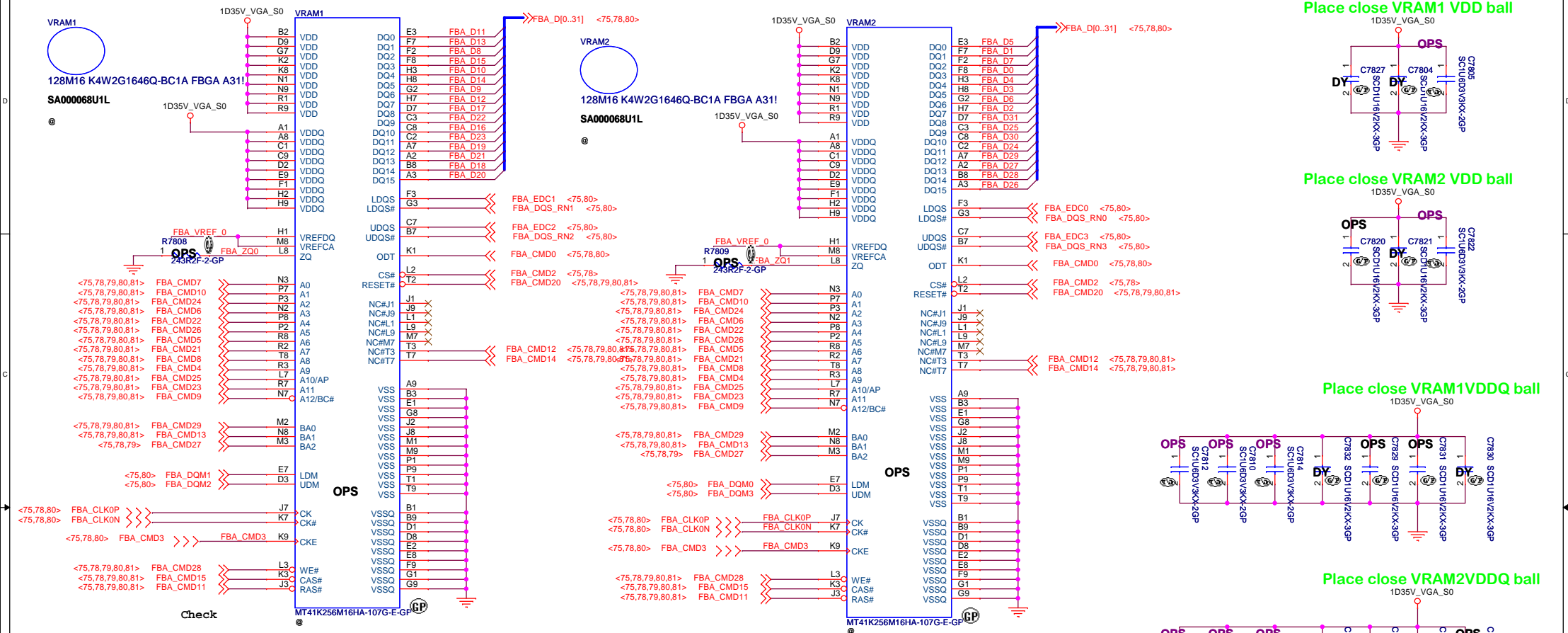
Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments
GB2B-64	4.7 $\mu$ F	X6S	0603	10	Under GPU
	1 $\mu$ F	X6S	0402	4	Under GPU
	47 $\mu$ F	X5R	0805	1	Near GPU
	22 $\mu$ F	X5R	0805	1	Near GPU
	4.7 $\mu$ F	X5R	0805	5	Near GPU
	330 $\mu$ F	POS	7343	1	Near GPU ESR $\leq$ 6 m $\Omega$



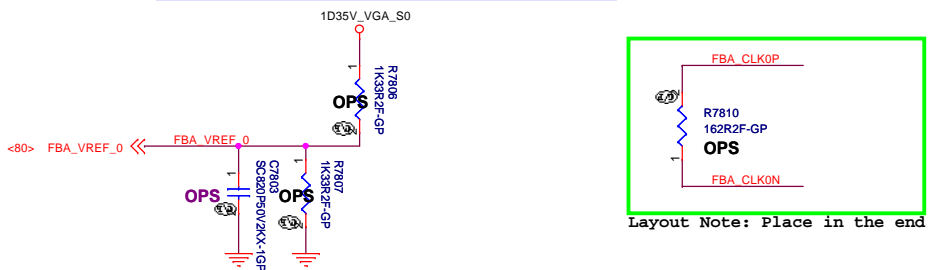
## Main Func = dGPU

## Data Bits 31:0 RANK 0



## Frame Buffer Partition A-Lower Half

## FBCLK Termination place on VRAM side



## FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

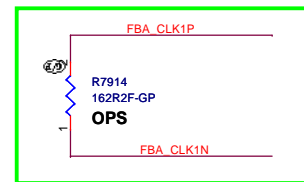
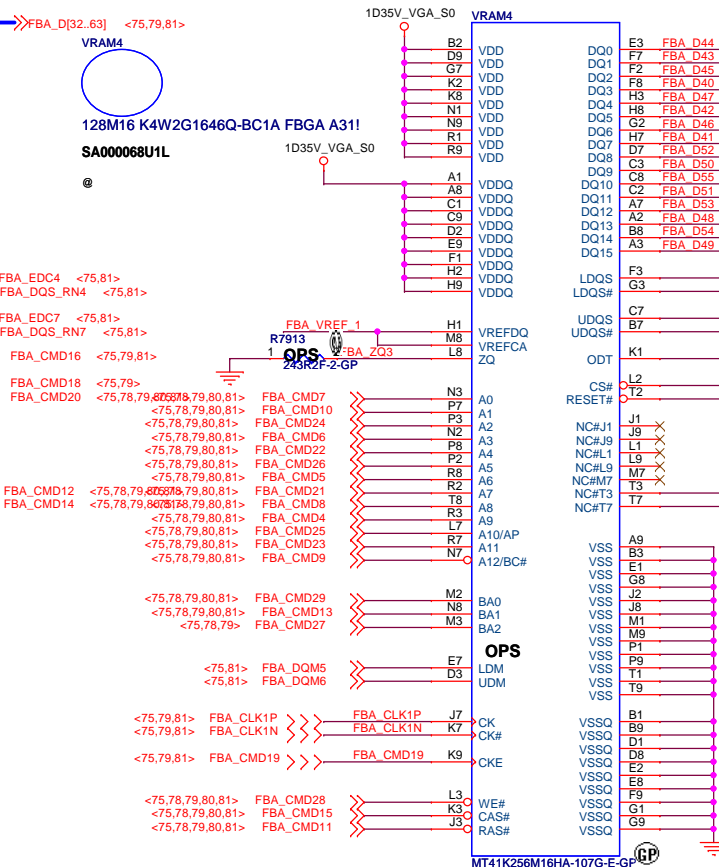
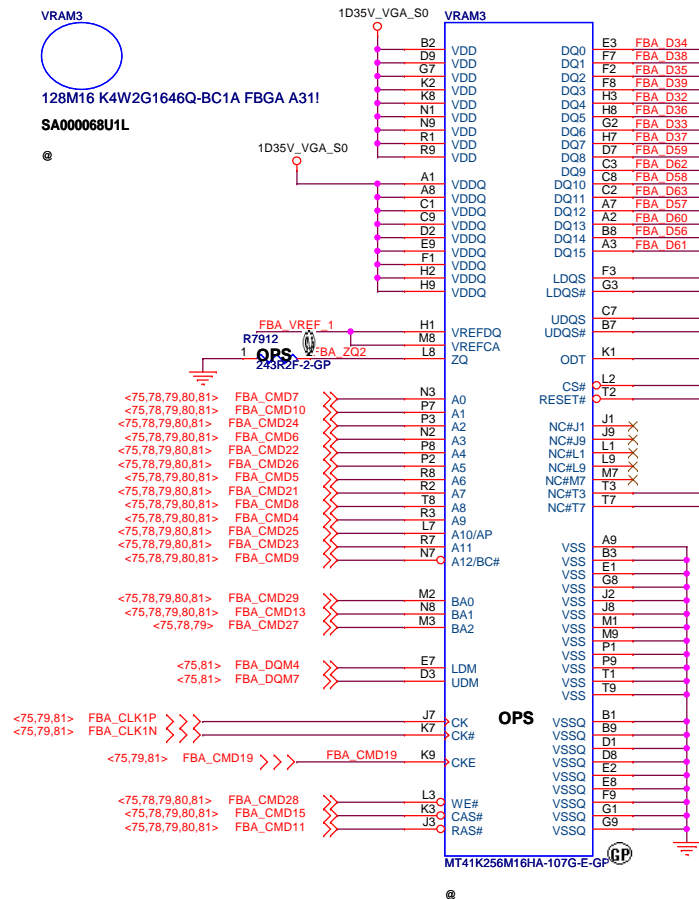
Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population		Location
			FBVDDQ	FBVDD	
FBVDD/Q Combined					
0.1 μF	X7R	0402	2		Under DRAM
1.0 μF	X7R	0603	4		Under DRAM
10 μF	X5R	0805	0		Close to DRAM

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Size	Document Number	Rev		Date		
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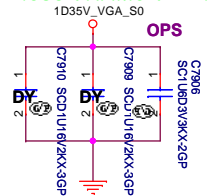
## Main Func = dGPU

## Data Bits 63:32 RANK 0

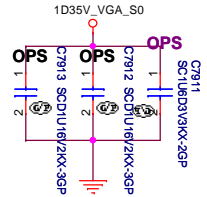


Layout Note: Place in the end.

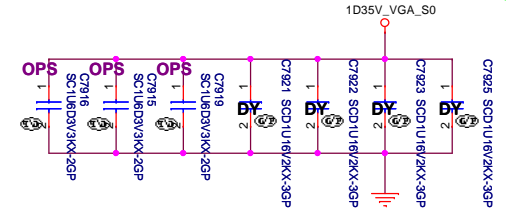
Place close VRAM3 VDD ball



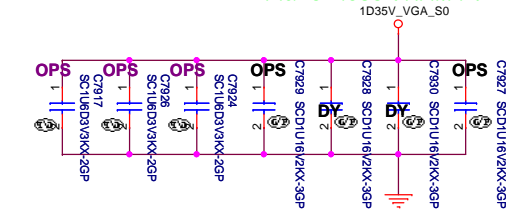
Place close VRAM4 VDD ball



Place close VRAM3 VDDQ ball



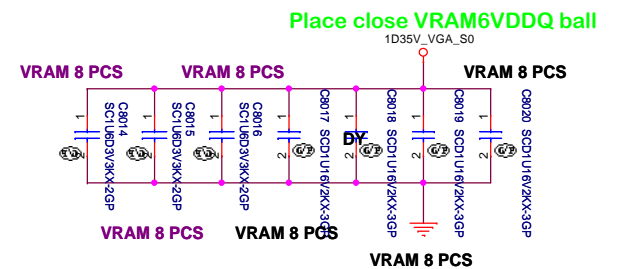
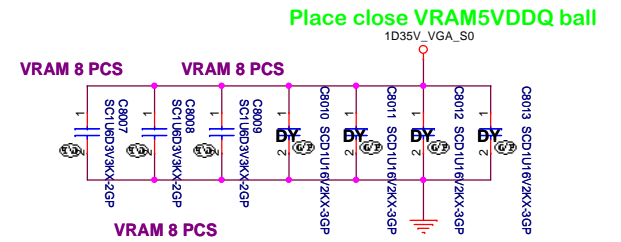
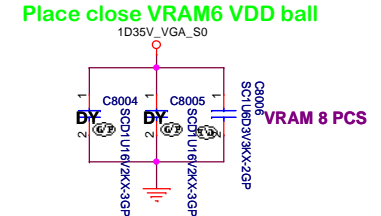
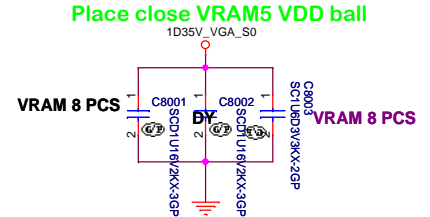
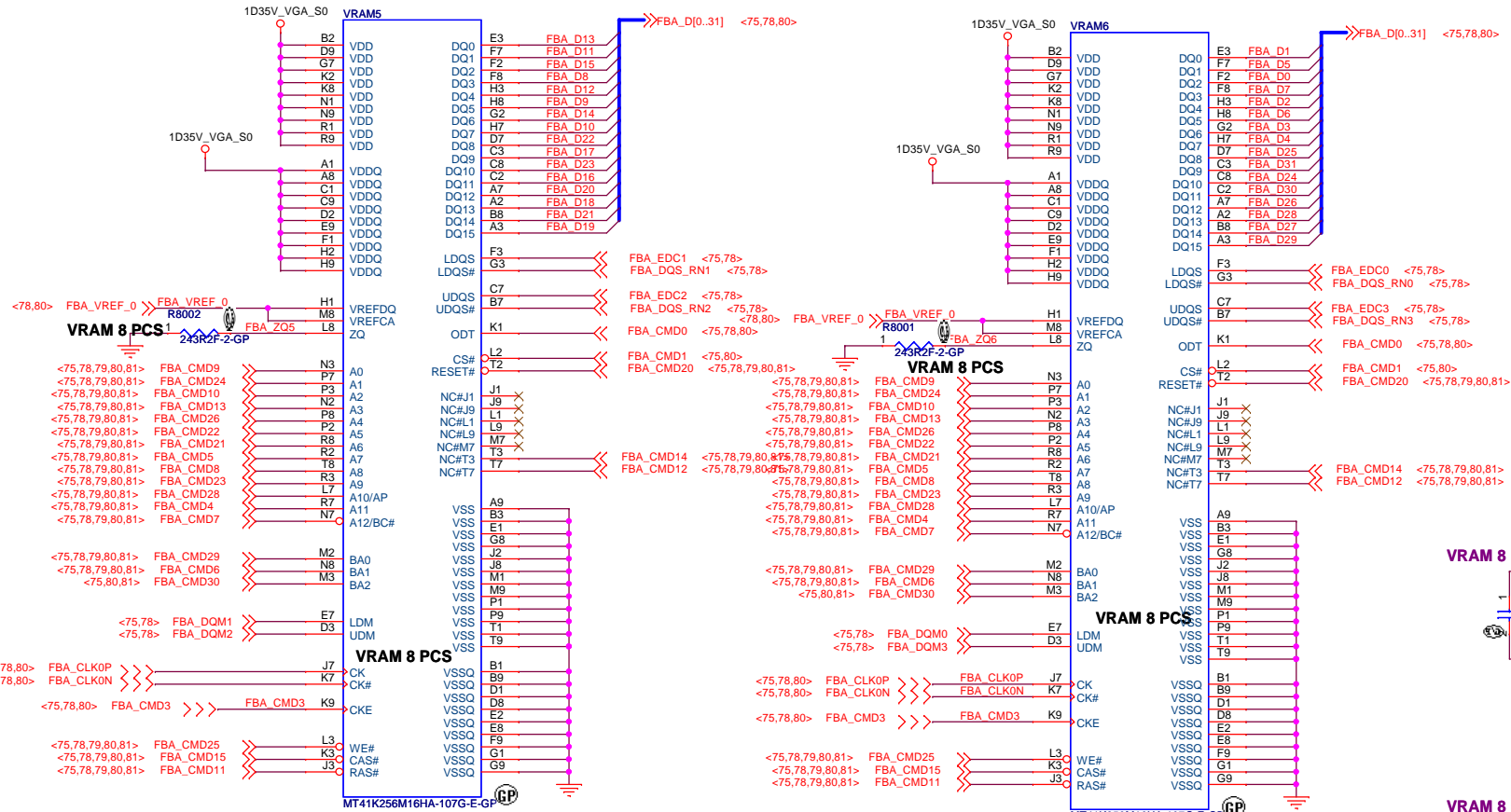
Place close VRAM4 VDDQ ball



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Main Func = dGPU

Data Bits 31:0 RANK 1



FBVREF Termination

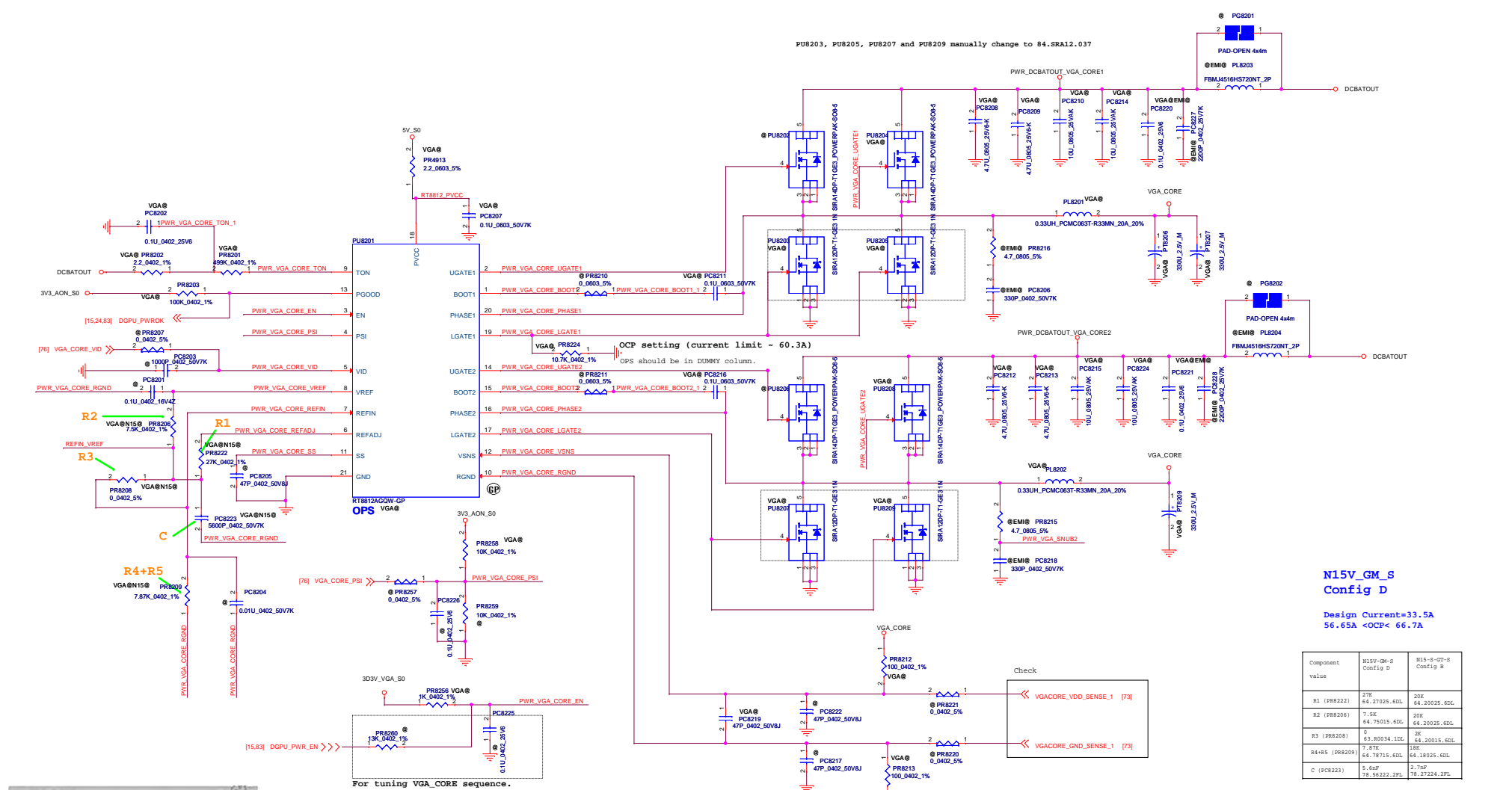
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

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PUB203, PUB205, PUB207 and PUB209 manually change to 84.SRA12.037



N15V\_GM\_S  
Config D

Design Current=33.5A  
56.65A <OCP< 66.7A

Component	N15V-GM-S Config D value	N15-G-0T-S Config A
R1 (PR8222)	27K 64.27025, 60L	20K 64.20025, 60L
R2 (PR8206)	7.5K 64.75015, 60L	20K 64.20025, 60L
R3 (PR8208)	0 63.80034, 10L	2K 64.20015, 60L
R4+R5 (PR8209)	7.87K 64.78715, 60L	18K 64.18025, 60L
C (PC8223)	5.6nF 78.56222, 29F	2.7nF 78.27224, 29F

78.56222, 29F: OMS REASON: 50V is more popular, change to 78.56224, 29F.

PWR-VID Specifications				
	Config A	Config B	Config C	Config D
Vmin	0.6	0.6	0.6	0.6
Vmax	1.2	1.2	1.15	1.15
Vboot	0.875	0.875	0.9	1.028
Voltage Step Width	mV	4.25	25	42.5
Number of Voltage Levels N	level	56	30	20
PWM Frequency F <sub>sw</sub>	MHz	1.125	0.876	0.876
PWM Minimum Pulse Width T <sub>min</sub>	ns	9.26	74	74
V <sub>D</sub> Transient Time T	-100	-100	-100	-100
Component Value				
R1 (R1)	KD	39	30	79
R2 (R2)	KD	39	30	7.5
R3 (R3)	KD	1.5	2	0
R4 (R4)	KD	30	18	24
R5 (R5)	KD	1.5	0	3
C	nF	1.5	2.7	5.6

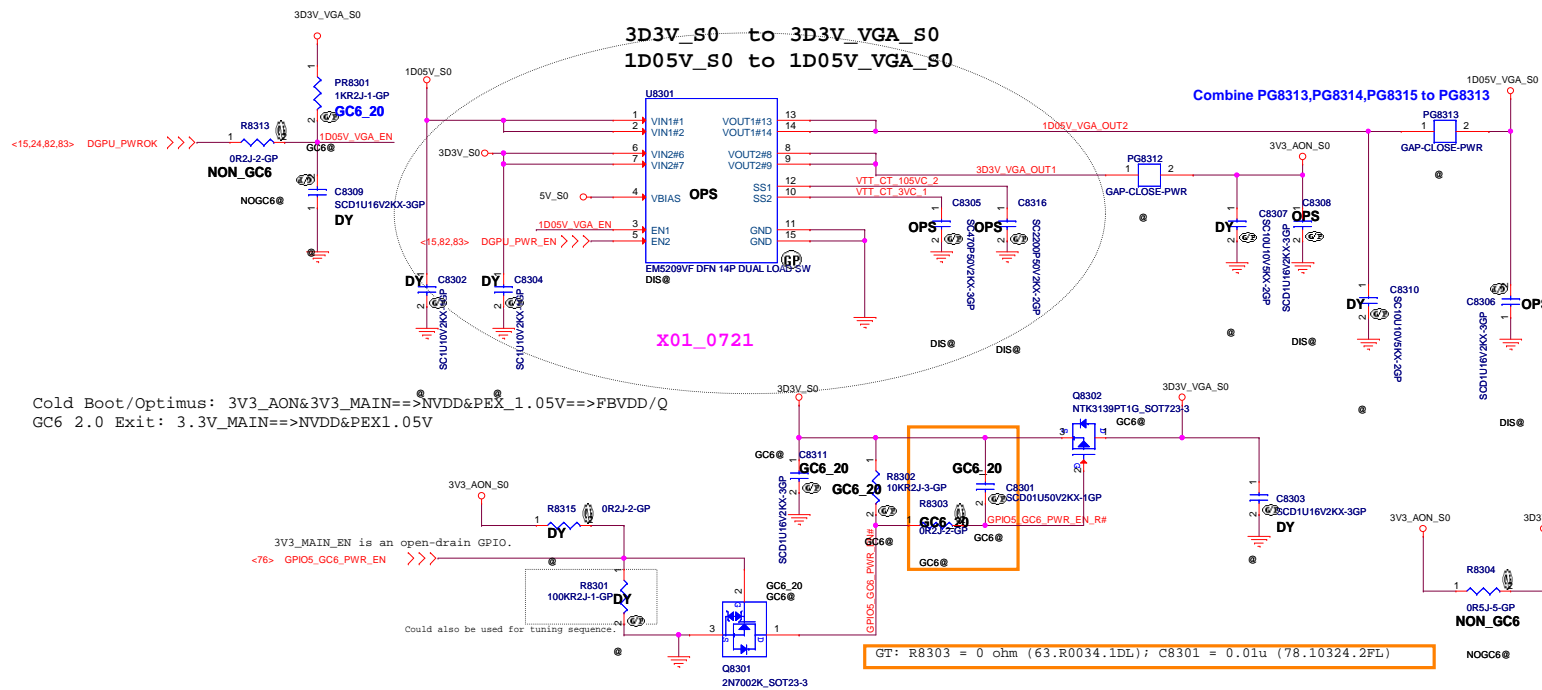


I/P cap: 10U 25V K0805 X5R/ 78.10622, 51L  
Inductor: CHIP CHOKE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C  
O/P cap: CHIP CAP EL 330U 2.5V M6.3\*4.4 Chemi-con/79.3371V.6CL  
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mohm@4.5Vgs/ 84.A14DP.037  
L/S: SIRA06DP-T1-GE3 / 2.75mohm/3.5mohm@4.5Vgs/ 84.SRA06.037

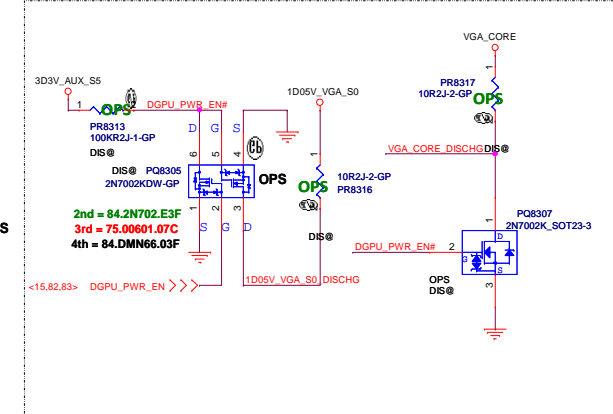
## Main Func = dGPU

3D3V\_VGA\_S0  
1D05V\_VGA\_S0

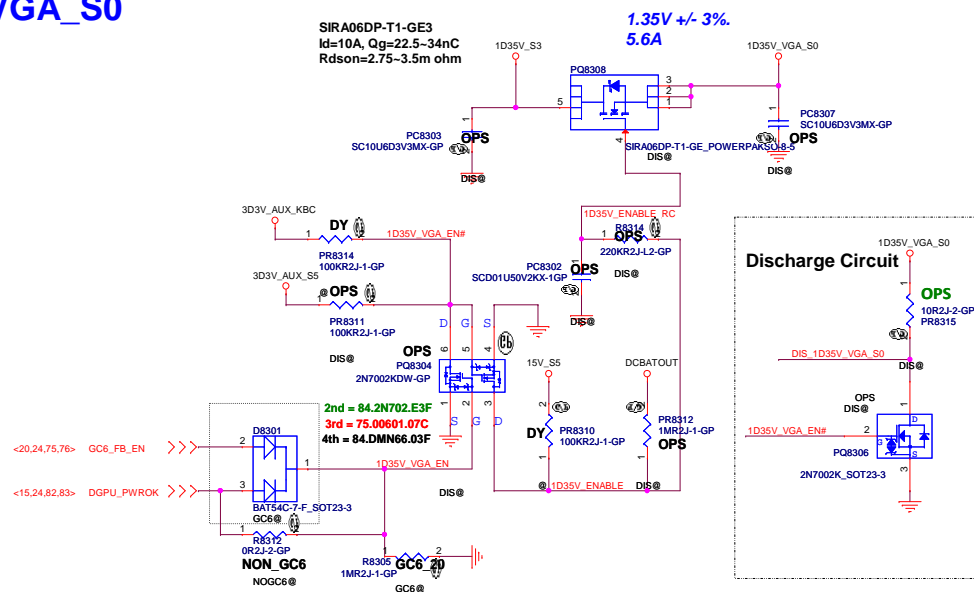
```
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0
```



### VGA\_CORE&1D05V\_VGA\_S0 Discharge Circuit



**1D35V\_VGA\_S0**



CTx (pF)	Rise Time (ns) 10% - 90%, COU = 0.1µF @ VIN; VOUT=0 ohm load							
	Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1, Rise time vs. CTx value

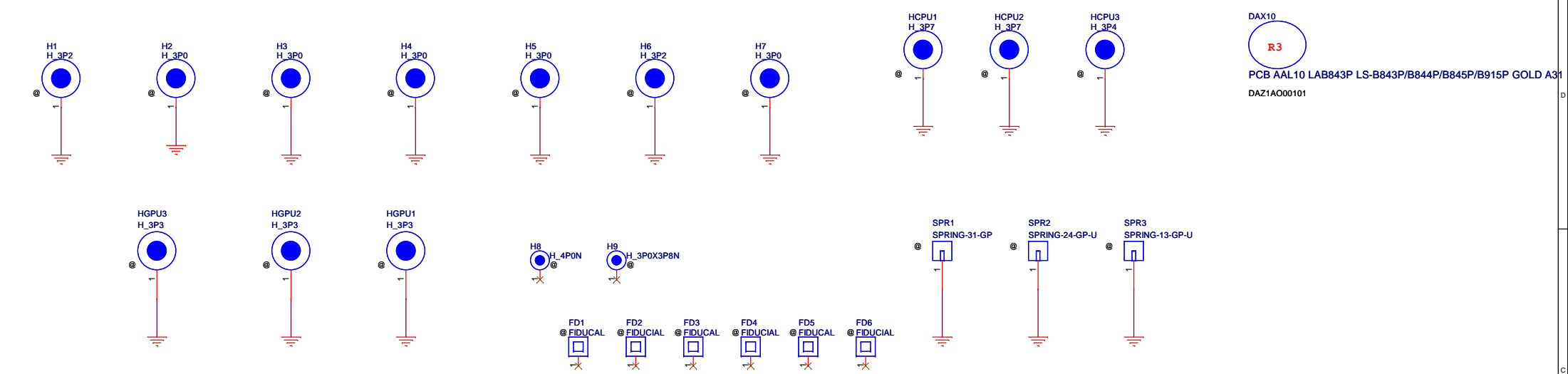
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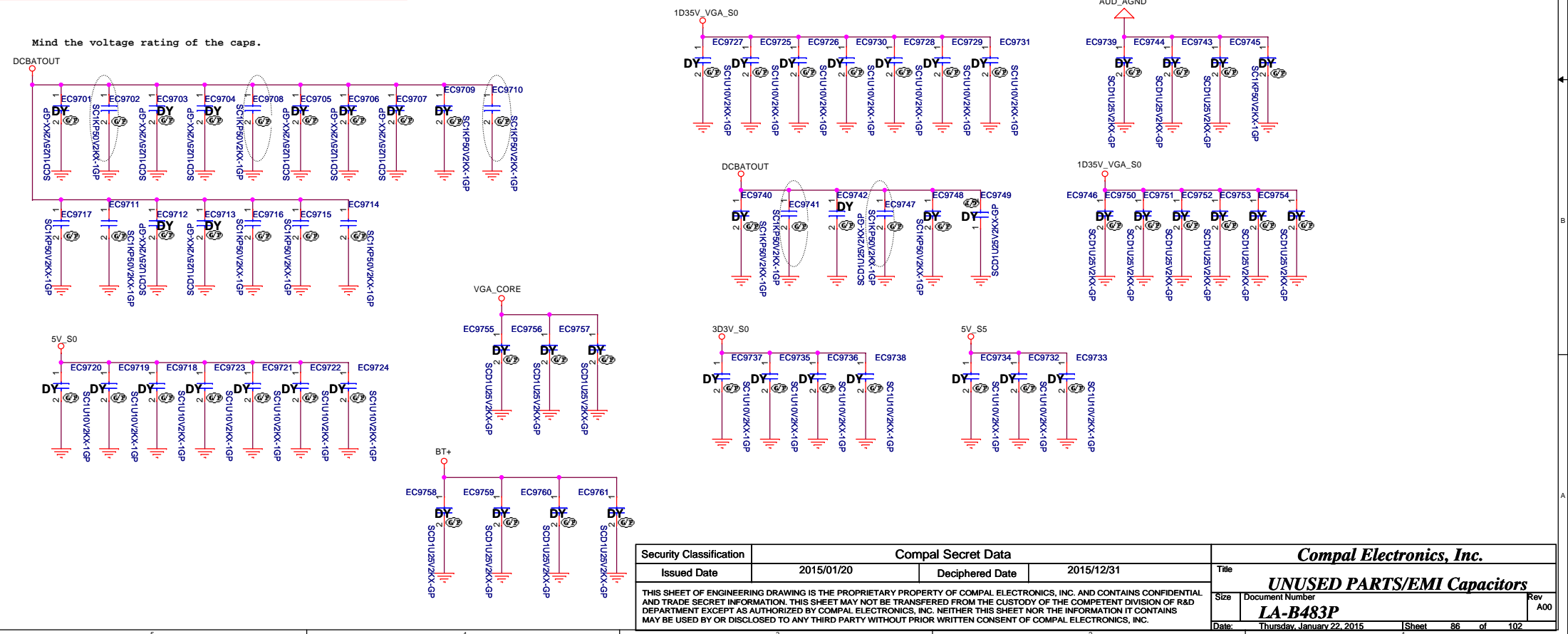
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Main Func = UnusedParts



Main Func = EMICapacitors



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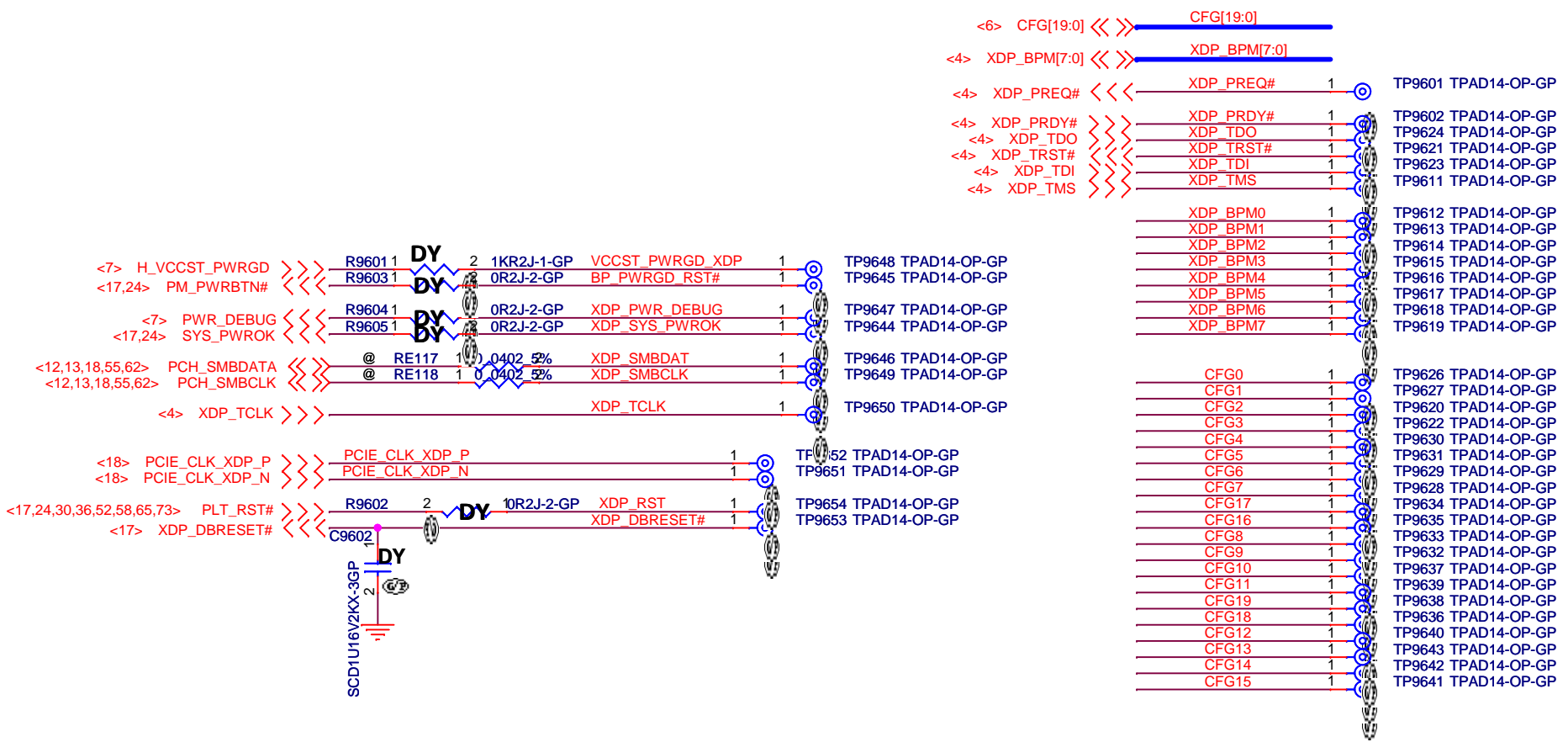
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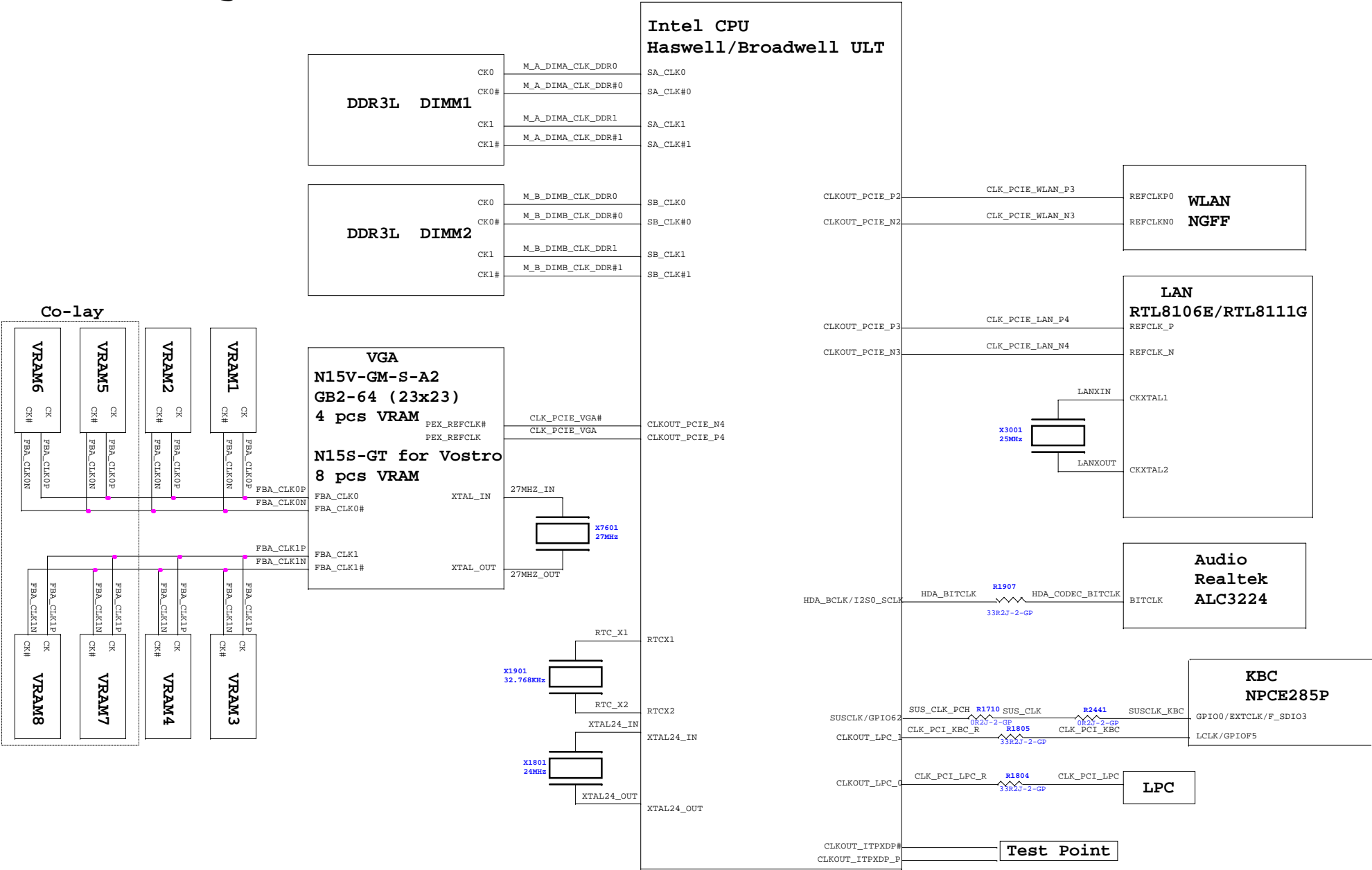
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CPU XDP





CLK Block Diagram



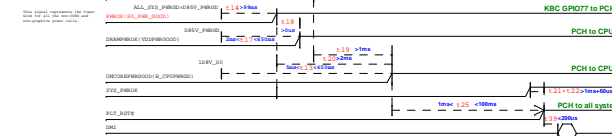
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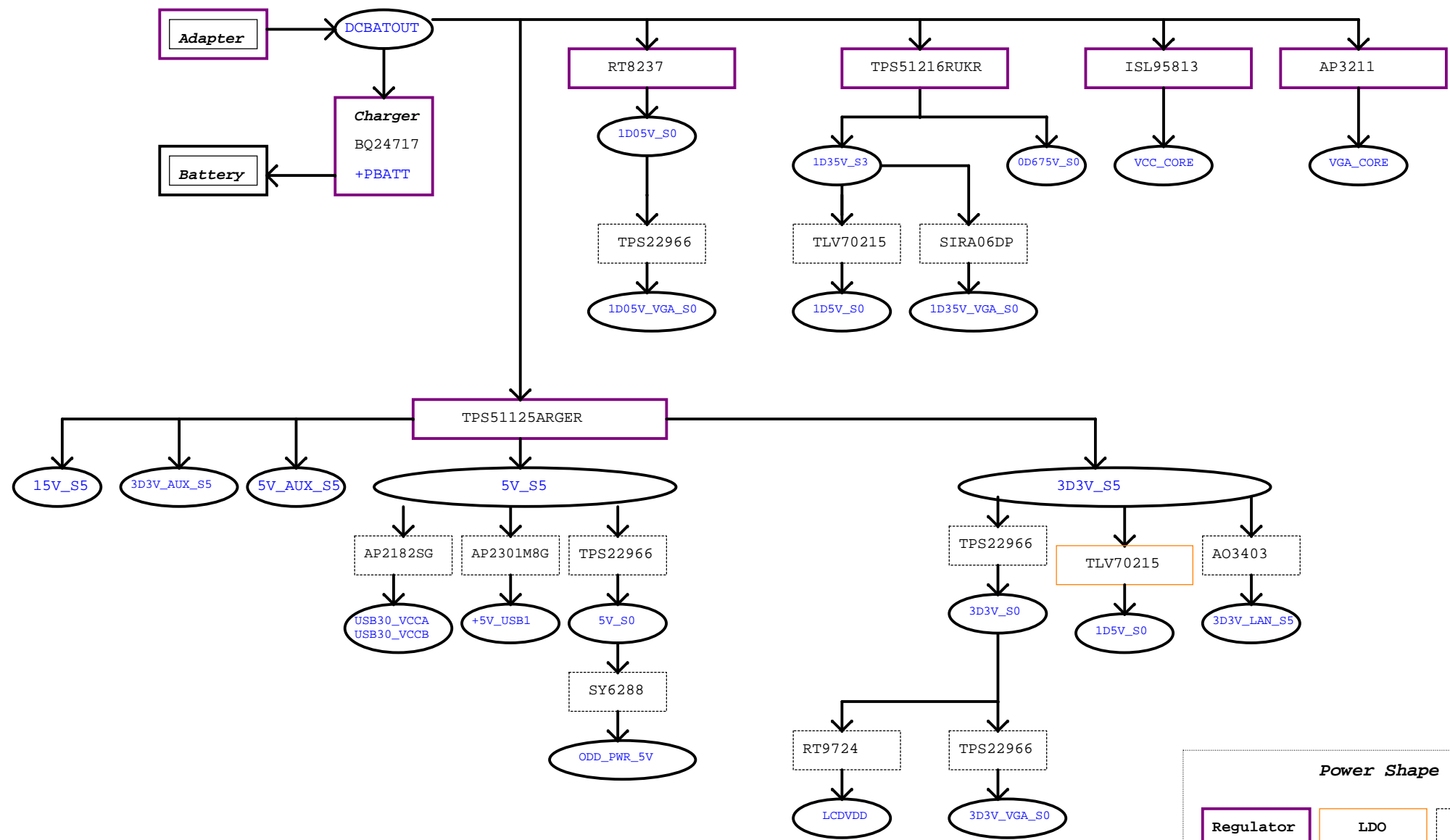
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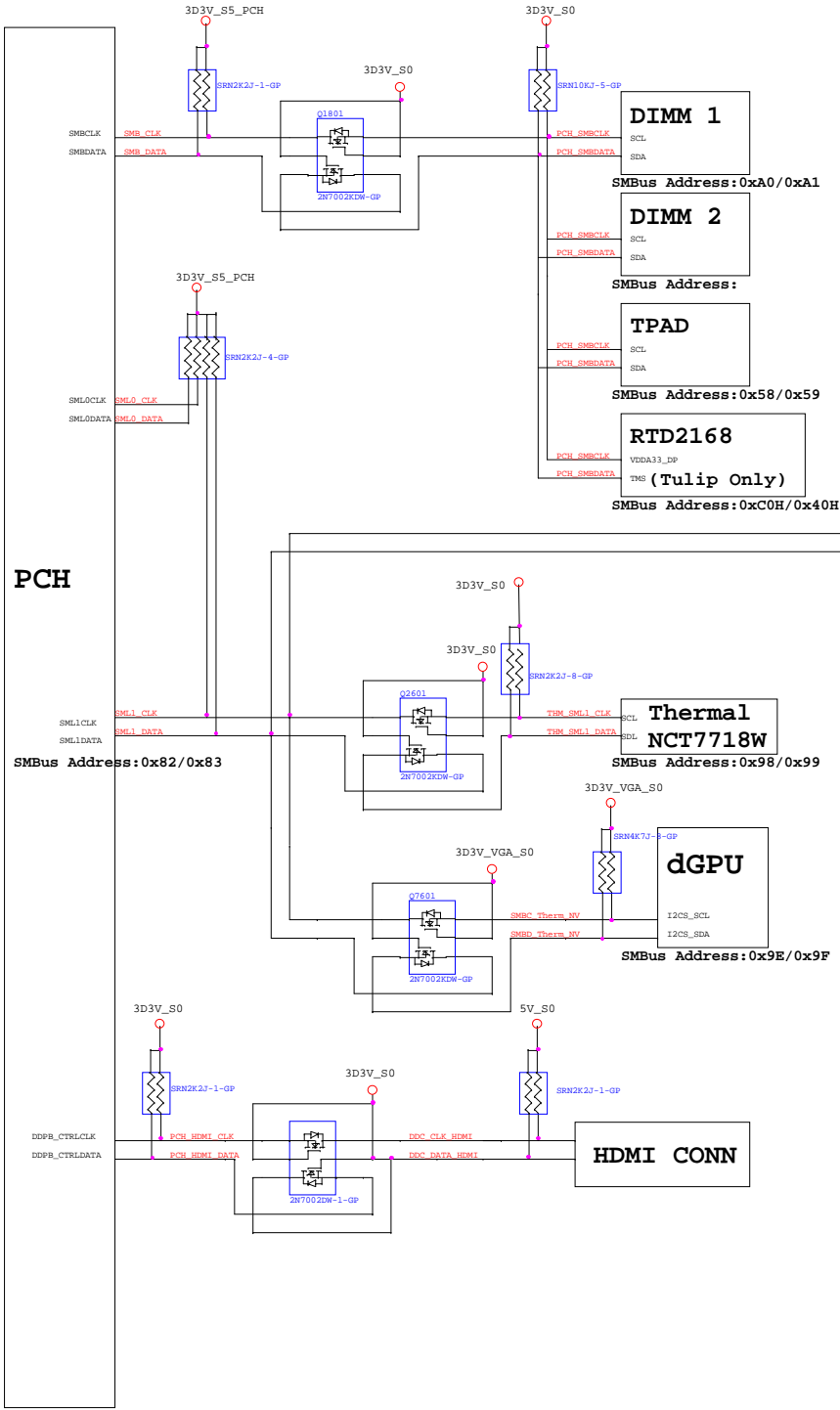




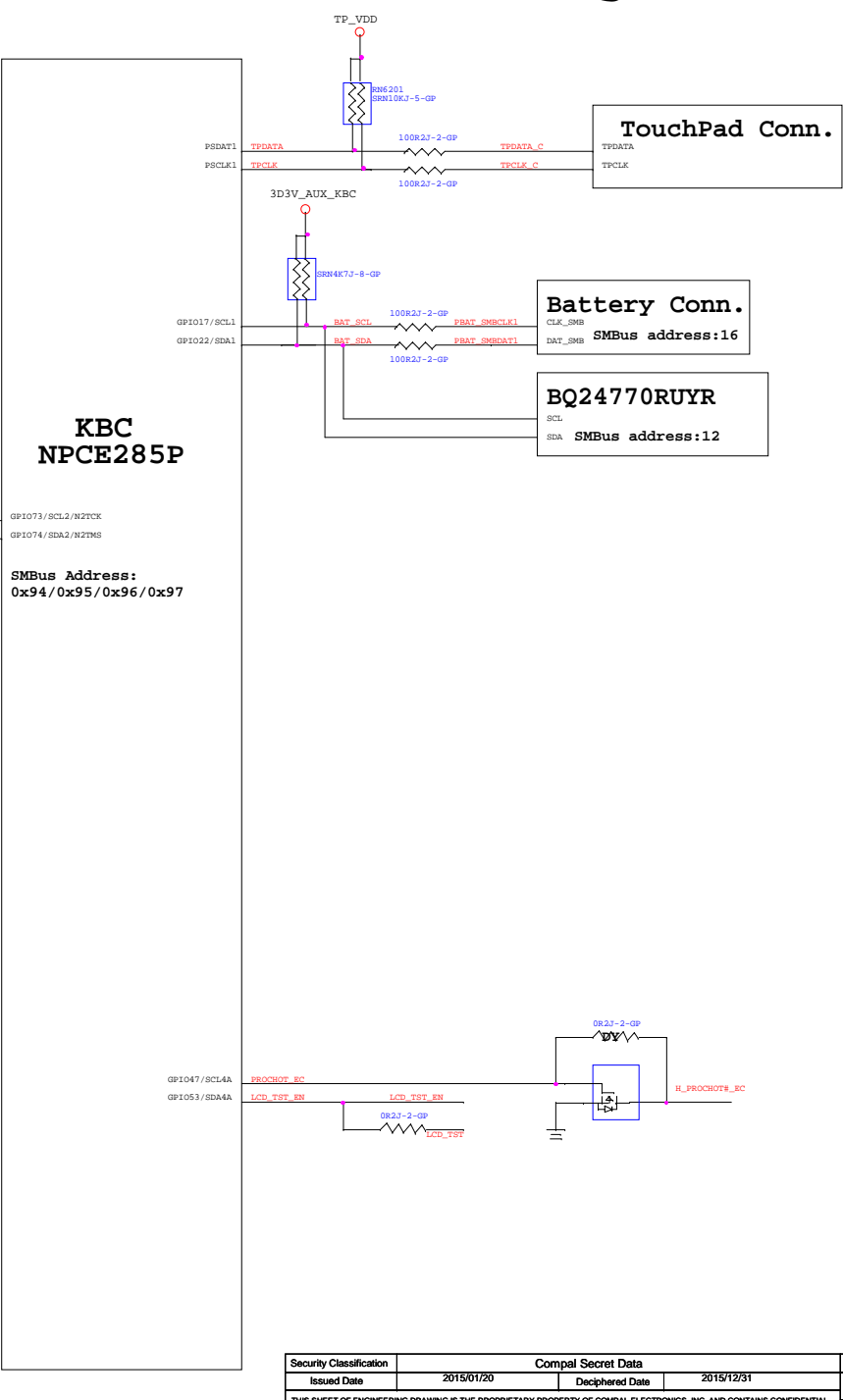
**Power Shape**

Regulator	LDO	Switch
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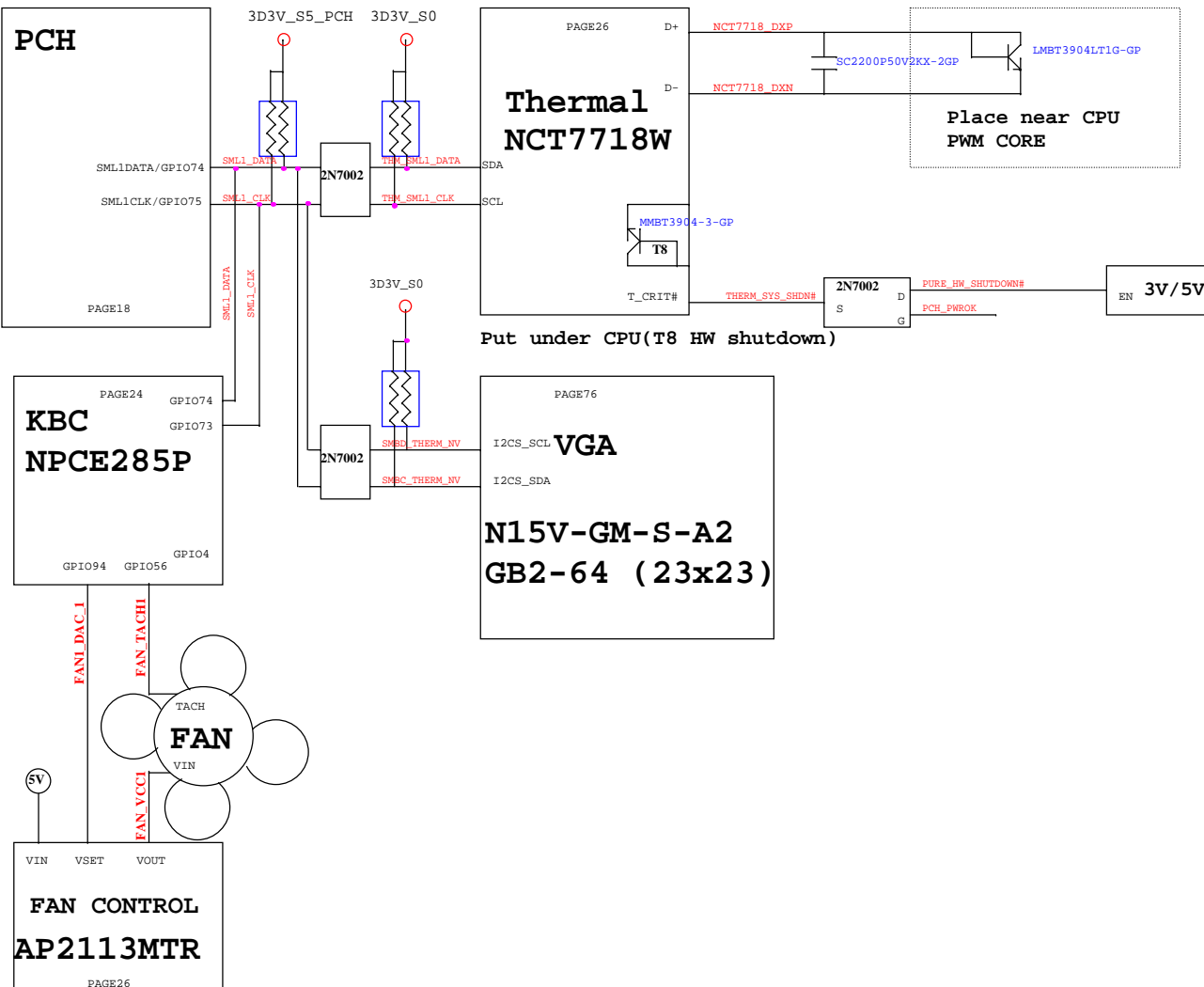
PCH SMBus Block Diagram



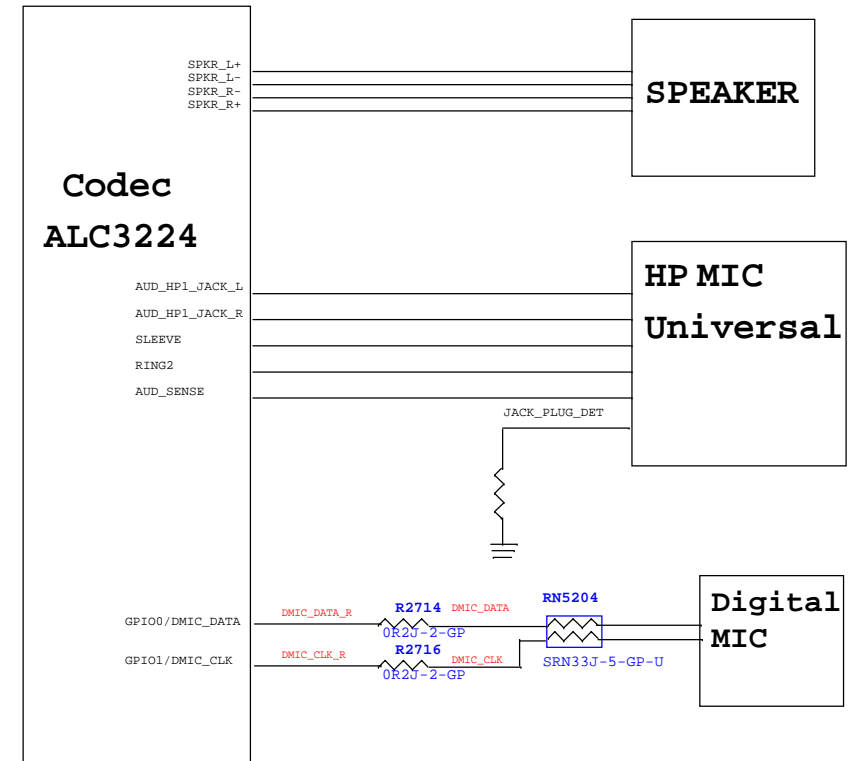
KBC SMBus Block Diagram



## Thermal Block Diagram



## Audio Block Diagram



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